

# 2.5D / 3D TSV & WAFER-LEVEL STACKING: TECHNOLOGY & MARKET UPDATES 2019

Market & Technology report - January 2019

*2.5D heterogeneous and 3D wafer-level stacking are reshaping the packaging landscape.*

## WHAT'S NEW

- Two main market segments:
  - High-end segment: high-performance computing, networking, gaming, and AR/VR/MR
  - Mid/low-end segment: CMOS Image Sensors (CIS), MEMS, and LED
- Semiconductor market mutation and its impact on stacking technologies
- Through silicon via's (TSV) extensive usage in HPC and networking hardware
- 3D System on Chip (SoC) technology to hit the market by 2019
- Hybrid bonding/stacking technology: markets, applications, forecasts, and players
- Stacking technologies forecast for the CIS market
- Technologies that are challenging 2.5D TSV interposer

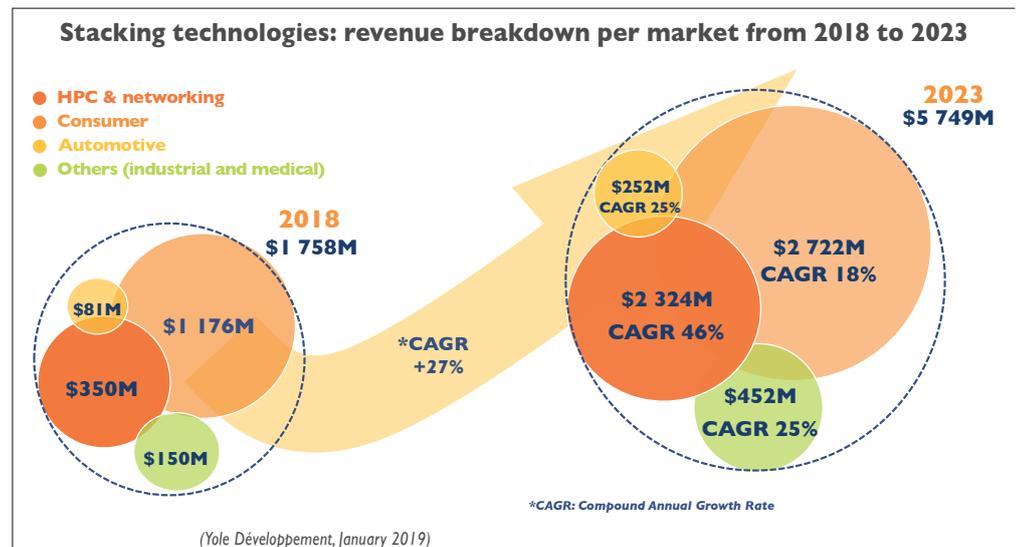
## KEY FEATURES

- Markets and applications requiring 3D stacking technologies
- High-end market segment: stacking technologies (TSV, 2.5D interposer, and 3D SoC), supply chain and forecasts for HPC, networking, gaming, and AR/VR/MR. Breakdown by product (stacked memory) and technology (2.5D and 3D SoC)
- Mid/low-end segment: technologies (TSV and hybrid bonding), supply chain, and forecasts for CIS, MEMS, sensors, and LED. Breakdown by technology for CIS and LED, and by application for MEMS & sensors
- The future of stacking technologies

## STACKING: ONE ALTERNATIVE FOR HIGH INTEGRATION BESIDE MOORE'S LAW

The slowdown of Moore's law opened the path to new inventions for answering actual mega-trends' stringent specifications. In the packaging field, 2.5D and 3D stacking technologies were preferred by many semiconductor players, and through silicon via (TSV) was the initial stacking technology. After several years of development and a focus on MEMS, it finally entered many applications. Today, 2.5D and 3D stacking technologies are the only solution that meet the required performance of applications like AI and data center as for today. Stacking technologies are used in a variety of hardware, including 3D stacked memory, Graphics Processing Unit (GPU), Field-Programmable Gate Array (FPGA), and CMOS Image Sensor (CIS), are intended for the high/mid and low-end market segments.

Hardware like High Bandwidth Memory (HBM) and CIS comprise the majority of TSV's revenue. The overall stacking technologies market will exceed \$5.5B in 2023 with a CAGR of 27%. As for today, the consumer market is the biggest contributor, with over 65% market share. But this, paradoxically, doesn't mean that consumer is the driver for these technologies. In reality, HPC is the real driver for stacking technologies and will exhibit the fastest growth up to 2023, with market share doubling from 20% in 2018 to 40% in 2023. In terms of packaging revenue, this equates to a more than 6x increase from 2018's revenue. Consequently, the consumer market's share will decrease. Other markets like automotive, medical, and industrial will maintain their current market share.



## FROM TSV TO WAFER-LEVEL STACKING, PACKAGING TECHNOLOGIES ARE FLOURISHING

Since the stacking battle is mostly between TSV-based and TSV-less technologies, these are the two categories Yole Développement considers in this report.

For today's high-end market segment, the most popular 2.5D and 3D integration technologies on the market are based on TSV for 3D stacked memory, and TSV interposer for heterogeneous stacking. Chip-on-Wafer-on-Substrate (CoWos) technology is already widely used for HPC applications, and new TSV technologies will hit the market in 2019, i.e. Foveros from Intel, which is based on "active" TSV interposer and 3D SoC technology, with hybrid

bonding and TSV interconnections (potentially). The Foveros example shows that although TSV is being challenged by non-TSV technologies, companies still have faith in it.

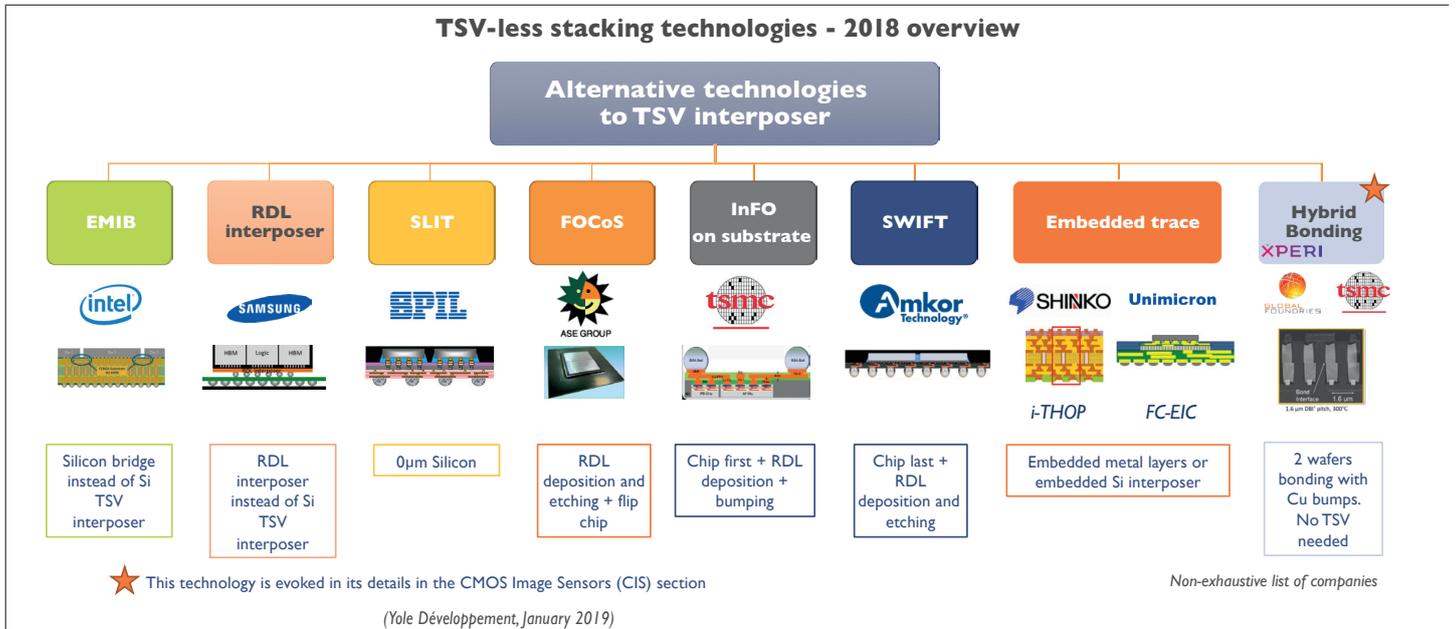
We cannot neglect the emergence of TSV-less technologies in the market. These innovations can be placed into two groups: "with substrate" and "embedded in substrate". Embedded Multidie Interconnect Bridge (EMIB) technology, already commercialized, is part of the embedded-in-substrate group, where the Si bridge is deep seating in the substrate. Other substrate technologies are being developed but are still not on the market, i.e.

Integrated Thin Film High Density Organic Package (I-THOP) and Flip Chip - Embedded Interposer Carrier (FC-EIC).

With-substrate technologies are also used as alternatives to TSV, for example InFO on substrate, which is widely used in Apple's processors. Also, redistribution layer (RDL) interposer technology is currently being developed and will hit the market by 2020. Last but not least, Fan Out Chip on Substrate

(FOCoS) was developed and commercialized in 2016, but seems to be lacking orders.

Hybrid bonding can bridge the two main categories (with TSV/without TSV). This technology's particularity is that it can be simultaneously TSV challenger and teammate. Since 2016 it has been commonly used in smartphones' CIS, and in the near future it will integrate the high-end market segment for memory and 2.5D as an interconnection solution.



### WHO IS BACKING AND CAPITALIZING ON STACKING TECHNOLOGIES?

Different players want their share of the growing \$5.5B stacking market, and four different business models are today locked in a race to win a piece of the stacking business: foundries, IDMs, OSATs, and IP companies.

Foundries like TSMC, UMC, and GlobalFoundries dominate TSV heterogeneous stacking technologies due to their ability to produce the interposer in-house. Intel, with its "Foveros" technology, is the only IDM trying to compete in this sector. For 3D stacked

memory, the battle is between the "Big 3" IDMs: Samsung, SK Hynix, and Micron. These companies will continue to reign over the stacked memory market. Meanwhile, 3D SoC is a foundry technology, and it is likely that only one foundry will manufacture it, in order to ensure high yield and limit risks. Here, TSMC leads the time-to-market race over GlobalFoundries.

For the TSV-less technologies, the game is a bit more engaged between foundries, IDMs, OSATs, and substrate makers. Some players, like Samsung, Intel,

### Overview of the main stacking technologies & players

Type	Company**	Technology name	With TSV	Without TSV	With Substrate	Without Substrate	Embedded in Substrate	Stacking technology
Foundry	      	CoWoS	★		★			2.5D
		InFO on substrate		★	★			
		3D SoC	★*			★		
IDM	    	3D stacked memory	★					3D
		RDL interposer		★	★			
		Foveros	★		★			
OSAT	  	FOCoS		★	★			2.5D
		SWIFT		★	★			
		SLIT		★	★			
Substrate manufacturer	 	i-THOP		★	★		★	2.5D & 3D
		FC-EIC		★	★		★	
IP		Hybrid Bonding	★	★	★	★		2.5D & 3D

\*3D SoC will use hybrid bonding & TSV may be required    \*\*Non-exhaustive list of companies

and TSMC, are involved in “with” and “without” TSV technology development. ASE (an OSAT) introduced its FOCoS technology to the market in 2016, while other players like Amkor have developed their proper technologies but are still awaiting orders.

Concerning substrate companies like Shinko, Unimicron, and most recently Fujitsu Interconnect, they are all still in R&D.

Xperi, an IP company, will positively impact the market because its hybrid bonding technology is midway between “with” and “without-TSV” technologies. Xperi’s other advantage is that its technology is compatible with both high and mid/low-end segments.

Foundries, IDMs, and IP companies have the advantage over OSATs in stacking technologies, since the latter encounter difficulties in obtaining orders.

**REPORT OBJECTIVES**

- Illustrate the impact of the semiconductor market’s mutation on packaging technologies
- Outline three stacking technologies: through silicon via (TSV), 3D system-on-chip, and hybrid bonding
- Provide an overview of the markets requiring stacking technologies, along with updated market data and forecasts
- Describe the hardware and key applications that are/will use stacking technologies
- Identify the main players and the supply chain for stacking technologies
- Reference nascent solutions that may challenge some of the existing stacking technologies
- Predict future applications where stacking technologies might be needed

**COMPANIES CITED IN THE REPORT (non exhaustive list)**

Alchip, Aledia, Alibaba, Amazon, AMD, Amkor, AMS, ANPEC, Apple, ASE, ASUS, Atos, Audi, Avago, Baidu, Bosch, Bitmain, BitFury, Broadcom, Canaan, Carsem, Cisco, Cray, DARPA, EBANG, EMmicroelectronic, EPworks, Facebook, Faraday, Fingerprints, Foxconn, Fraunhofer, Fujitsu, Gigabyte, GlobalFoundries, Google, GUC, HalongMining, HLMC, HP, Huatian, Huawei, I Biden, IBM, Icsens, IMEC, Inari Technology, Infineon, Innosilicon, Intel, InvenSense, JCET STATS ChipPAC, Juniper, Lenovo, Leti, Lfoundry, LGInnotek, mCube, Melexis, Memsic, Mercedes-Benz, Micralyne, Micron, Microsoft, NEC, Nokia, Nvidia, NXP, Omnivision, ON Semiconductor, OpenSilicon, Osram, PTI, Samsung, SensL, Shinko, SK Hynix, SMIC, Sony, SPIL, STMicroelectronics, Tencent, TF, Toshiba, TPK, TSMC, UMC, Unimicron, Xfab, Xilinx, Xintek, XMC, Xperi, YMTC, and more...

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**AUTHOR**



**Mario Ibrahim** is a member of the Semiconductor & Software division at Yole Développement (Yole), working as a Technology & Market Analyst for advanced packaging. Mario develops technology & market reports and produces custom consulting studies. He is also deeply involved in test activity business development within the division. Prior to Yole, Mario specialized in test activity development for LEDs at Aledia. He also headed several R&D advanced packaging programs. During his five-year stay at Aledia, Mario developed strong technical and managerial expertise in different semiconductor fields. Mario holds an Electronics Engineering degree from Polytech Grenoble (France). He apprenticed for three years in the Imaging division of STMicroelectronics Grenoble, where he contributed to the testing and benchmarking of automation advancements within the test & validation team.

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Branch code: 00170  
Account n°: 0170 200 1565 87  
BIC or SWIFT code: CCFRFRPP  
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