The demand for lower cost plus higher performance, coupled with OSAT/assembly house end-customers' desire for increasingly lower prices, has driven the semiconductor industry to develop innovative solutions. One approach to reducing overall cost is to switch from wafer and strip-level to a larger-size panel format that takes advantage of efficiency and economies of scale. Going from wafer to panel (for example 12" wafer to 18" x 24" panel) could enable cost reductions of up to 50% (if technologies are ready) and yields exceeding 90%. Panel-level manufacturing has the potential to leverage the knowledge and infrastructure of wafer-level packaging (WLP) and the PCB/flat-panel display/photovoltaic industries.

Various factors are driving Panel Level Packaging (PLP) development and encouraging diverse players from across the supply chain (including equipment and materials) to invest in panel infrastructure. On one side, the leading fabless players want OSATs to reduce the cost of high-density FOWLP and going to large size panel is seen as the key step to significantly reducing the package price. In fact, FOPLP is on every big OSAT’s roadmap. On the other side are players whose strategy is to invest and develop PLP capability and push hard for its adoption. These players, mainly driven by the success and publicity surrounding FOWLP, are also those that:

- Missed the early FOWLP (eWLB) wave (i.e. PTI, ASE)
- Were affected by losses in the substrate business and want a new business model that utilizes their experience in substrate manufacturing (i.e. SEMCO, Unimicron)
- Already have experience in panel processes (i.e. LCD packaging) and believe they can leverage this experience for PLP (i.e. NEPES)
- Want to develop high-density, low-cost packaging to support their front-end chip business (Samsung Electronics, Intel)

**WHAT'S NEW**

- Updated 2017 - 2023 Panel Level Packaging (PLP) forecast, by packaging platform
- Updated, in-depth analysis of potential applications that could drive the PLP business
- Update on the activities of the various players involved in PLP
- Updated “Equipment and Materials” section: in-depth coverage of the processes, tools, and materials for PLP, as well as technical challenges, key suppliers, and competitive benchmarking
- Equipment suppliers’ PLP-specific strategies
- Different players’ PLP technology development, readiness, and adoption time
- Comprehensive analysis of the various manufacturing challenges for PLP adoption
- Revised technology roadmap (based on the 2017 - 2023 high volume manufacturing technology roadmap)

**KEY FEATURES OF THE REPORT**

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- Overview of panel packaging technologies that are available or in-development: FOWLP panel and embedded die
- Commercialization status, market adoption, and potential for each packaging technology
- Drivers and challenges for technology adoption
- Per-player product/technology description and analysis
- Detailed supply chain, market adoption roadmap, and volume forecast for each panel platform
- Panel adoption and panel equipment readiness roadmap
- Equipment and materials challenges

**WHY IS THE INDUSTRY INTERESTED IN PANEL LEVEL PACKAGING?**

**TECHNOLOGY**

- Form factor / Thin profile
- High electrical/thermal performance
- High components integration
- Design flexibility
- Physical protection

**APPLICATION**

- Mobile / IoT / Wearables
- Automotive
- Computing
- Medical

**COST**

- Higher efficiency and economies of scale
- Higher carrier usage ratio >95%
- Benefit for large package size
- Wafer to panel FO ~ 50% less cost

**MARKET DRIVERS FOR PANEL LEVEL PACKAGING PLATFORMS**

- Leverage experience of substrate manufacturing
- New business model
- Enter the fan-out business
- Leverage experience of FPD/PCB/PV expertise
- High density, low cost package solution to support front-end business

**STRATEGIC MOVE**

- Enter the fan-out business
- New business model
- Leverage experience of FPD/PCB/PV expertise
- High density, low cost package solution to support front-end business

**SUPPLY CHAIN: STATUS AND READINESS**

Many packaging platforms can be considered panel-based, but for this report we consider only two packaging technologies to be PLP, where both RDL interconnect fabrication and further assembly are done at panel level (with panel size >300 mm x 300 mm): FOPLP and embedded die. Between the two, FOPLP is the most-discussed and the one which attracts the greatest interest of many players (including equipment and suppliers), and thus is the main focus of this report.

Lots of players have been developing FOPLP technology, but after years of development/qualification/sampling, three players will finally enter in production in 2018: Powertech Technologies (PTI), NEPES, and SEMCO. NEPES has been in low-volume production since 2017. ASE, in partnership with Deca Technologies, is in the advanced development stage and will commence volume production in 2019/2020. Each player has its own business strategy and is working on its own FOPLP technology (panel size, leveraging...
Different criteria must be fulfilled and certain challenges overcome for FOPLP’s broad adoption. These criteria/challenges are linked to large capex investment, standardization, multisource availability, and most importantly, market availability to keep the panel line running. There are technical challenges too, such as warpage control, die placement accuracy, and the fabrication of sub 10/10um line, etc. on large panels. Standardization of the panel size and assembly process is the biggest hurdle for FOPLP adoption. Each player is developing its own process using different panel sizes and infrastructure (PCB/LCD/WLP/PV/Mix) catering to specific applications and customers. In this scenario it’s very difficult for end-customers to multisource. Also, it’s not profitable for equipment suppliers to design and manufacture equipment according to different customers’ requirements.

Given the technical challenges that will adversely affect the yield, the FOPLP that go into HVM production will support a relatively simple design: >10/10 umL/S, <10 x 10 mm² package size, Max 2L RDL. With the maturation of the technology and the experience gained, FOPLP will eventually be adopted for high-density design with <10/10um L/S, multi-layer RDL, >15 x 15mm² package size, and multi-die SiP integration.
OBJECTIVES OF THE REPORT
• Provide an overview of panel package technologies
• Describe the key applications that could use the panel infrastructure
• Highlight panel package solutions and the players supporting these packages
• Identify the current and future industrial players for each packaging technology, based on panel level
• Provide market data and forecasts for panel products
• Explore each segment’s competitive landscape

COMPANIES CITED IN THE REPORT (non exhaustive list)

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ROADMAP: VOLUME PRODUCTION FOR FAN-OUT PANEL LEVEL PACKAGING

<table>
<thead>
<tr>
<th></th>
<th>2018</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
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<tbody>
<tr>
<td>Minimum die-to-die distance</td>
<td>250µm</td>
<td>200µm</td>
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<td>Minimum bump pitch</td>
<td>400µm</td>
<td>350µm</td>
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<tr>
<td>Maximum die size</td>
<td>15mm</td>
<td>12mm</td>
<td>15mm</td>
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<tr>
<td>(X–Y directions)</td>
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<tr>
<td>Minimum die size</td>
<td>900µm</td>
<td>500µm</td>
<td>200µm</td>
<td></td>
</tr>
<tr>
<td>(X–Y directions)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package minimum thickness</td>
<td>250µm</td>
<td>200µm</td>
<td>150µm</td>
<td></td>
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<tr>
<td>(without BGA)</td>
<td></td>
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<td></td>
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<tr>
<td>Line/Space</td>
<td>15/15µm</td>
<td>10/10µm</td>
<td>8/8µm</td>
<td>5/5µm</td>
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<tr>
<td>Maximum level of RDL</td>
<td>2RDL</td>
<td></td>
<td>3RDL</td>
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<tr>
<td>Maximum package size</td>
<td>8*8mm</td>
<td>10*10mm</td>
<td>15*15mm</td>
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</tbody>
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ROADMAP: VOLUME PRODUCTION FOR FAN-OUT PANEL LEVEL PACKAGING

(Yole Développement, April 2018)

EXECUTIVE SUMMARY

Find more details about this report here.
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