

DIE ATTACH EQUIPMENT MARKET 2019

Market & Technology Report - October 2019

Growing business and new technical challenges are ensuring consolidation of the die attach equipment market.

KEY FEATURES

- Market and technology trends in the die attach equipment market
- Die attach equipment business investigations through various segmentations:
 - > By bonding technologies, such as mass reflow, TCB, eutectic, solder, sintering, epoxy, hybrid bonding
 - > By different device applications, such as logic, memory, RF, MEMS, CIS, discrete, LED, optoelectronics/photronics
- In depth analysis of the die bonder and flip-chip bonder market
- Comprehensive list of die attach equipment suppliers with over 70 companies identified
- Technological roadmap and benchmarking of the equipment covering various devices and technologies
- Supply chain analysis: overview of the key equipment suppliers across various segments along with the installed base at their customers
- Merger and acquisition trends in the die attach equipment business
- Competitive landscape of key tool suppliers

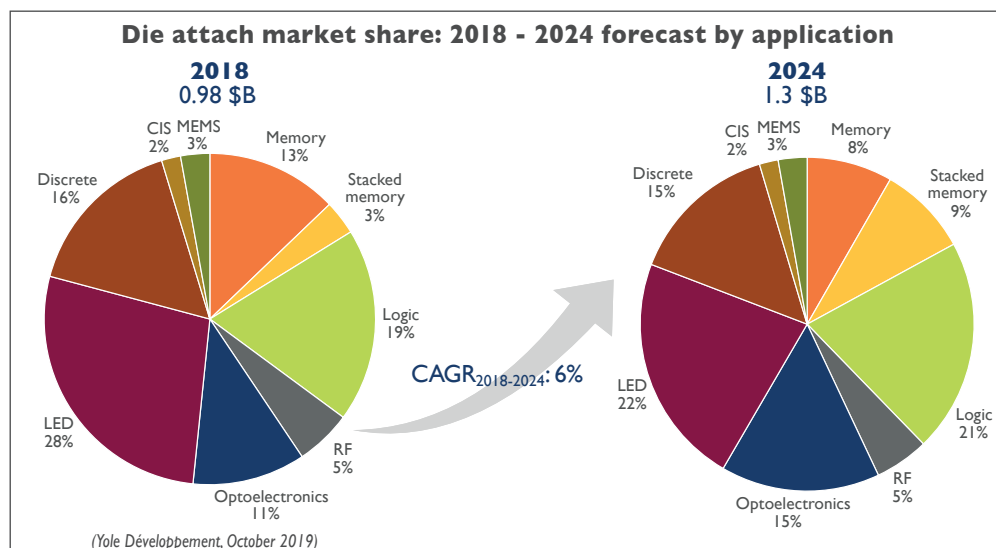
THE DIE ATTACH EQUIPMENT MARKET WILL HAVE A 6% CAGR, REACHING \$1.3B BY 2024, FUELLED BY ASSEMBLY AND PACKAGING OPPORTUNITIES CREATED BY SEMICONDUCTOR MEGATRENDS

Today's semiconductor megatrends include mobile devices, big data, artificial intelligence (AI), fifth generation (5G) wireless networking, high performance computing (HPC), the internet of things (IoT) including industrial IoT, smart automotive, industry 4.0, and data centres. These applications create demand for electronics hardware, which requires high computing power, high speed, more bandwidth, low latency, low power, more functionality, more memory, system level integration and a variety of sensors. Such trends create business opportunities across various electronic device packaging platforms. However advanced packaging has one of the best opportunities, as it can fulfil various performance and complex heterogeneous integration requirements.

Die attach is a key process step in semiconductor packaging. It covers all devices across various applications and is a key contributor to assembly cost. The die attach equipment business will benefit from assembly and packaging opportunities created by the above-mentioned trends. Die attach equipment can be classified into two categories: die bonders and flip-chip (FC) bonders. The total market was worth \$979M in 2018 and is expected to grow at 6% CAGR from 2018-2024 to reach \$1.3B. The FC bonder market will grow with a 12% CAGR to reach \$290M in 2024 whereas the die bonder market will grow with a 5% CAGR to reach \$1.09B in 2024.

By application, the highest growth is in stacked memory bonder market, with a 24% CAGR, followed by optoelectronics, with a 12% CAGR, and logic, with an 8% CAGR.

In terms of technology, epoxy bonding dominates die attach for wire-bond packaging, and related die bonders constituted around 85% of the total bonder market in 2018. However, epoxy bonding's share will reduce to 53% by 2024. Eutectic bonding growth is driven by MEMS, high power light emitting diodes (LEDs) and optoelectronics applications. Chip-to-wafer (C2W) hybrid bonding is the emerging promising technology that can enable direct Cu-Cu bonding and has potential to replace TCB for the 3D stacked memory and high end logic application. However C2W hybrid bonding is still in its early stages level and is expected to hit the market in 2021 for stacked memory and in 2022/23 for logic devices with 2.5D structures. The Die Attach Equipment Market Report 2019 will cover the die attach equipment business in detail including market forecasts, player market shares by different technologies, and application segmentations. In this report, more than 70 equipment suppliers are identified across various geographical locations. The different applications covered are logic, memory, RF, MEMS, CIS, discrete, LED, optoelectronics etc. The various die attach technologies include mass reflow, TCB, eutectic, solder, sintering, epoxy and hybrid bonding.



HETEROGENEOUS INTEGRATION ENABLED BY ADVANCED PACKAGING AND 3D STACKING IS PUSHING THE DEVELOPMENT OF NEXT GENERATION DIE ATTACH EQUIPMENT

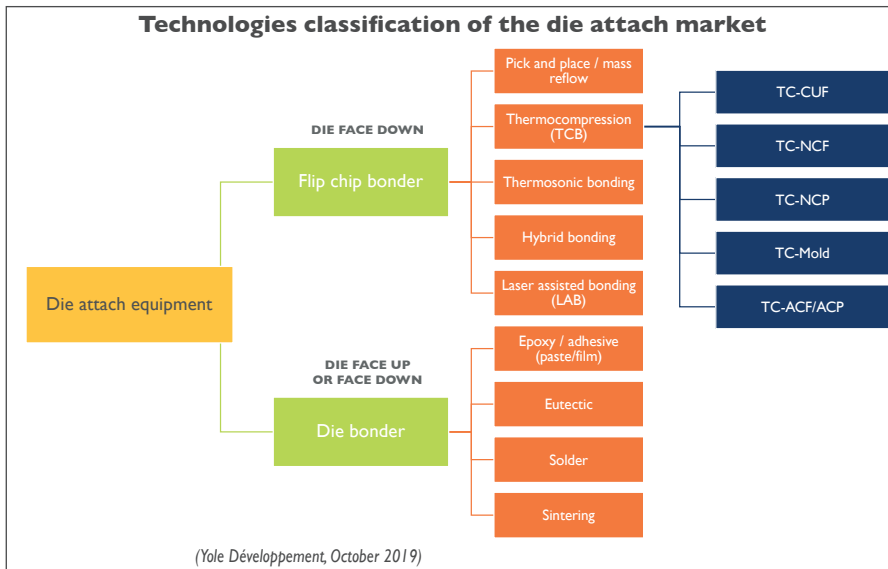
Currently the main flip-chip bonding technology is mass reflow, followed by TCB. Different types of TCB exist, and each is more or less dedicated to a certain type of application: TC-NCF, TC-NCP, TC-CUF, TC-Mold, TC-ACF/ACPLow unit-per-hour (UPH) rates are the key bottleneck for adoption of TCB in various applications. Equipment suppliers are using various methods, such as tool design and improved processes, to increase UPH rates.

To support the ultra-fine pitches below 20µm and high-density interconnect, new tools needs to be developed. They must have high accuracy (<3µm at both global and local level),high speeds (>5,000 UPH), allow multi-mode operation to support different bonding processes, parallel pick up with more than four dies, with both flip and non-flip capabilities, have advanced inspection capabilities, a wider process window, able to

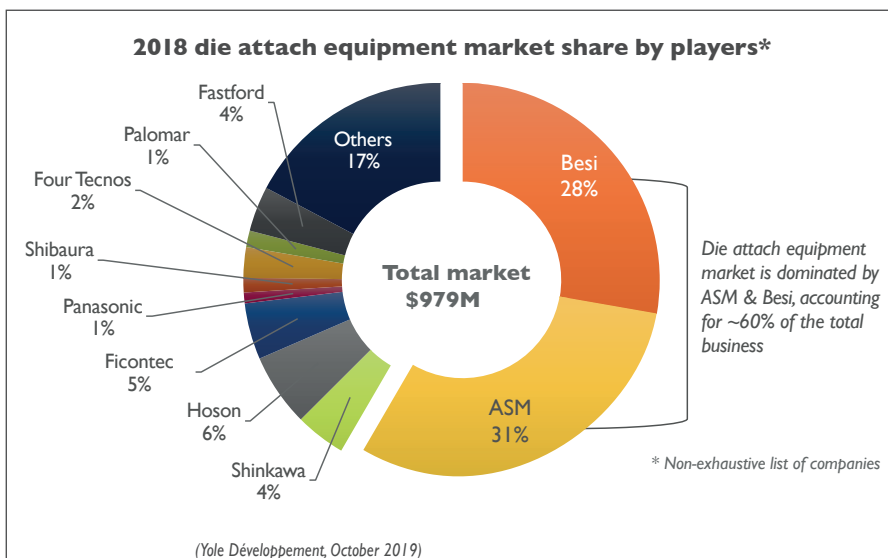
handle large die sizes, large panel die bonding for areas above 600mm x 600mm etc.

As mentioned above, epoxy/adhesive bonding is the main die bonding method, with eutectic bonding growth driven by MEMS, high power LED and optoelectronics applications. Soldering is the main die-attach technology for power devices. Sintering is an emerging technology that will replace soldering in power devices in future. To achieve high memory density, die stacking using wire-bonding is still the main technology for NAND flash packaging. It will remain the dominant technology in the coming years. Die Attach Film (DAF) is an ultra-thin film adhesive used to connect multiple dies in die-attach processes for flash memory. Ultra-thin die handling and cleanliness before die stacking are two main challenges for NAND flash packaging for die attach bonders. Flip-chip copper pillar adoption is increasing for DRAM for the PC and server applications.

Die-to-wafer hybrid bonding is an emerging technology that can replace TCB-NCF processed in 3D TSV memory. Existing tools that are compatible with such technology can be used to validate this approach. Next-generation hybrid bonding tool challenges also include surface cleanliness and die handling. Laser Assisted Bonding (LAB) is a new interconnect technology that could replace mass reflow processes for fine-pitch flip-chip bonding. It uses heat from a laser to wet out the areas between die bumps, substrate pads and other components. This report covers the technology trends, challenges, and requirements of die attach tools in different applications and packaging platforms in detail.



THERE IS INCREASING CONSOLIDATION AMONG DIE ATTACH EQUIPMENT SUPPLIERS



Although there are lot of companies involved in producing flip-chip and die attach bonders, just a few players dominate the various application segments. Two players, Besi and ASM, dominate the bonder business. They account for more than 50% of the market. This is because bonders are their main businesses, while bonders are a small part of the other players' businesses. Other key players are Shinkawa, Shibaaura, Panasonic, Toray and Hanmi. Fastford is active in memory packaging, especially NAND flash. Hoson is the leader in LED packaging in the Chinese market. Four Tecnos, Ficontec and Palomar are mainly involved in the optoelectronics packaging tool business.

There is consolidation going on in the assembly equipment business. Players are diversifying their

tool offerings to support various business segments and assembly processes through mergers and acquisitions (M&As).

The report investigates competitive landscape of key tool suppliers, M&A trends in detail, various scenarios, the players' competitiveness, and discusses who will win and lose.

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AUTHOR

Santosh Kumar is currently working as Principal Analyst and Director Packaging, Assembly & Substrates, Yole Korea. Based in Seoul, Santosh is involved in the market, technology and strategic analysis of the microelectronic assembly and packaging technologies. His main interest areas are advanced IC packaging technology including equipment & materials. He is the author of several reports on fan-out / fan-in WLP, flip chip, and 3D/2.5D packaging. Santosh Kumar received the bachelor and master degree in engineering from the Indian Institute of Technology (IIT), Roorkee and University of Seoul respectively. He has published more than 40 papers in peer reviewed journals and has obtained 2 patents. He has presented and given talks at numerous conferences and technical symposiums related to advanced microelectronics packaging.

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CONTACTS

- For more information about :
- Consulting & Financial Services: Jean-Christophe Eloy (eloy@yole.fr)
 - Reports & Monitors: David Jourdan (jourdan@yole.fr) & Fayçal Khamassi (khamassi@yole.fr)
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