Everspin EMD3D256M Memory

256Mb Spin Transfer Torque MRAM

SP20543  - Memory report by Belinda Dube
          Physical analysis done by Nicolas Radufe

June 2020 - Sample
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Executive Summary

This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of Everspin’s EMD3D256M STTMRAM.

Amongst multiple emerging NVM technologies, spin transfer torque magneto resistive RAM (STT-MRAM) has shown significant potential and market growth driven by low latency storage applications. In 2018 MRAM Market recorded a Revenue of $44 million dollars. Compound annual growth rate of MRAM market is estimated at 85% between 2018 and 2024.

Magnetoelectronic memories have been employed in numerous information devices because of their nonvolatile characteristics, high speed and low power consumption. Their high endurance characteristic has made the STT MRAM Memory a good competitor in the memory industry and promises to pick up significant market shares in the next few years.

Everspin’s STT MRAM component has a compact structure integrating numerous layers that include ferromagnetic material and antiferromagnetic material forming a magnetic tunnel junction. Different resistive states created in the MRAM memory cell allow read and write functions. A dielectric layer is coupled between two magnetic materials. A complex fabrication method is used to deposit and pattern the thin layers that form the STT MRAM memory cell.

Everspin Technologies leads the (STT-) MRAM market. The 256Mb STT MRAM memory uses a 40 nm technology node. The memory is manufactured along with the CMOS Transistors.

System Plus Consulting presents a deep analysis of Everspin’s EMD3256M STT MRAM Memory. The report includes an Analysis of the package and the dies, the MRAM memory cell and focusing on the layered material that make up the MRAM Cell memory. It also features a cost analysis and a price estimation of the component; this cost analysis integrates the manufacture of the CMOS transistors and the MRAM Memory cells. The manufacturing process steps are detailed including the supply chain. The results of manufacturing cost are used to determine the cost per Mb for Everspin’s STT MRAM Memory.
The reverse costing analysis is conducted in 3 phases:

**Teardown analysis**
- Package is analyzed and measured
- The dies are extracted in order to get overall data: dimensions, main blocks, pad number and pin out, die marking
- Setup of the manufacturing process.

**Costing analysis**
- Setup of the manufacturing environment
- Cost simulation of the process steps

**Selling price analysis**
- Supply chain analysis
- Analysis of the selling price
PHYSICAL ANALYSIS
Package Opening - Wire Bonding

- **Wire Bonding**
  - Material: 
  - Wire number: 
  - Wire Diameter: 
  - Wire average length: 

[Image: Memory Package Opening]
Die Cross-Section – Substrate Thickness

Die Cross-Section – Optical View

Die Cross-Section – SEM View

- Die substrate thickness: μm.
The MRAM Cell junction is located between the layer.

connect the MRAM cell structure to the copper metal layer.
Die Cross-Section – MRAM Cells

- The cross section reveals
- The MRAM Memory cells are placed

In-line MRAM Cells
(MRAM Cells not in the same plane. (The two cells are placed...)

Die Cross-Section - SEM View
©2020 by System Plus Consulting
Die Cross-Section – MRAM Cells

- Copper interconnects require into the dielectric layer.
- The layers layer are deposited before electroplating copper.
- The layers

**Die Cross-Section - SEM View**
©2020 by System Plus Consulting
Die Cross-Section – MRAM Cells
### Die Cross-Section – MRAM Cells

<table>
<thead>
<tr>
<th>Material (estimated thickness)</th>
<th>MRAM Cell Part</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiN Al2O3</td>
<td>Encapsulating layers</td>
<td>protects MRAM layers from subsequent etching operations. May protect the layers from degradation.</td>
</tr>
<tr>
<td>Ta (8nm)</td>
<td>Top Electrode</td>
<td>Electrode</td>
</tr>
<tr>
<td>MgO</td>
<td>Capping Layer/Spacer</td>
<td>allows containment of the and the SAF structure</td>
</tr>
<tr>
<td></td>
<td>Top Magnetic Material</td>
<td>Free Magnetic layer</td>
</tr>
<tr>
<td>MgO</td>
<td>Tunnel Barrier</td>
<td>Dielectric layer that provides diffusion barrier</td>
</tr>
<tr>
<td></td>
<td>Coupling Layer</td>
<td>Fixed ferromagnetic</td>
</tr>
<tr>
<td>CoPt (1.2nm)</td>
<td>Pinned layer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pinning layer</td>
<td>Determines orientation of the MRAM cell</td>
</tr>
<tr>
<td></td>
<td>Seed layer</td>
<td></td>
</tr>
<tr>
<td>Ta</td>
<td>Bottom Electrode</td>
<td>Electrode</td>
</tr>
</tbody>
</table>

Die Cross-Section – SEM View

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Layer identified using EDX. Thickness is a close estimation.
Die Process – Memory Cells

- After removing the top metal layers the MRAM Cells are exposed.
- The MRAM Cells are ______ the top view.
- ______ material penetrates the MRAM memory cells.
- The MRAM Cells have ______.
Die Process – Memory Cells

Vertical Cross Section reveals the MRAM Memory cells:

- MRAM Cell pitch
- MRAM Cell width
- Smallest distance between two MRAM Cells
- This corresponds to technology node
Die Delayering – Memory Cell Density

Area of 1 memory block:
\[
\text{Area of 1 memory block} = \text{mm}^2
\]

Area measured contains 8 memory cell blocks and non memory cell:
\[
\text{Area measured} = \text{mm}^2
\]

- Memory cell area in measured area:
\[
\text{Memory cell area} = \text{mm}^2
\]

- Area occupied by memory cells on the measured area:
\[
\text{Area occupied by memory cells} = \% \text{ of the die area.}
\]
Die Process – Memory Cell Size

Area of 1 Memory block = \( \text{mm}^2 \)

Number of memory block cells on Die = \( \text{cells} \)

Total MRAM Cell area on die = \( \text{mm}^2 \times \text{cells} = \text{mm}^2 \)

MRAM Cell Size/Area = \( \frac{\text{mm}^2}{\mu m} = \text{\mu m}^2 \)

Total/Maximum number of MRAM Cells in Die = \( \text{mm}^2 \times \mu m^2 = \text{MRAM Cells} \)

Full/Maximum Memory Capacity = \( \text{Mb} \)

MRAM Memory Die Density
• Active Area on die = \( \text{mm}^2 \)
• Memory density in active area = \( \text{Mb/mm}^2 \)
STT MRAM Memory Process Steps

- CMOS creation
- Creation of Metal 1 to Metal

- PECVD SiN
- PECVD SiO2

- Pattern and etch
  - Lithography 1
  - Deposit
  - PVD
  - CMP
STT MRAM Memory Process Steps

- Pattern and etch SiO sides Lithography
- Deposit encapsulation

- Pattern and etch Al2O3 encapsulation (top layers) Lithography

- PECVD SiO layer
- Pattern and etch SiO2
- Deposit
- PVD
- CMP
C O S T
ANALYSIS
STT MRAM Memory - CMOS & Metal Layers Front-End Cost

<table>
<thead>
<tr>
<th>CMOS transistor + 5 Metal layers</th>
<th>Q2 2020</th>
<th>Q3 2020</th>
<th>Q4 2020</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Raw wafer Cost (Si 300mm)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clean Room Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equipment Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Consumable Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Labor Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The CMOS and Metal layers **front-end cost** for the MRAM Memory ranges from $150 to $250 according to yield variations.

The largest portion of the manufacturing cost is due to the **Raw wafer Cost**.
STT MRAM Memory Cells Front-End Cost

<table>
<thead>
<tr>
<th>MRAM Memory Cell</th>
<th>Q2 2020</th>
<th>Q3 2020</th>
<th>Q4 2020</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield Losses Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Memory (CMOS, Metals, MRAM Cells) Front-End Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Foundry Gross Profit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Memory (CMOS, Metals, MRAM Cells) Front-End Price</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The **front-end cost** for the STT MRAM Memory Cells ranges from [insert range here] according to yield variations.

The largest portion of the manufacturing cost is due to the

We estimate a **gross margin of** [insert percentage here] for GlobalFoundries, which results in a **front-end price** ranging from [insert range here].
The component cost is estimated at between low and high yield. The die cost accounts for of the cost (for medium yield). The packaging represents % of the total component cost (for medium yield). Final Test and yield losses represent % of the total component cost (for medium yield).
We estimate that Everspin Technologies realizes a gross margin of  on the MRAM Memory, which results in a final component price ranging from  

This corresponds to the selling price for large volume to OEMs.
Related Reports

**MEMORY REPORTS**

- Intel Optane 128GB DIMM
- 3D NAND Memory Comparison 2019
- LPDDR4 Memory Comparison 2019

**MEMORY REPORTS**

- Emerging Non-Volatile Memory 2020
- MRAM Technology and Business 2019