

THINNING EQUIPMENT TECHNOLOGY AND MARKET TRENDS FOR SEMICONDUCTOR DEVICES

Market & Technology Report - June 2020

Memory, CIS, and power applications are driving the wafer thinning equipment market, before a new wave of innovation by 2025.

KEY FEATURES

- Comprehensive analysis of the major applications currently using thinning methods, and potentially attractive applications that could require the use of different thinning technologies in the future
- Describe the key benefits and added value of thinning technology in the semiconductor field
- Thinning technology by device roadmap
- 2019-2025 thinning equipment market forecast: breakdown by device type, by substrate type and by equipment technology
- Describe the competitive landscape and identify key players in technology development
- 2019 global thinning equipment market share in the field of semiconductor
- Discuss technology processes, specifications, and supply chain

DEMAND FOR THINNED WAFERS IS GROWING CONSIDERABLY, DRIVEN BY MINIATURIZATION, ALONG WITH GREATER PERFORMANCE OF SEMICONDUCTOR DEVICES

The demand for thinned wafers continues to increase owing to miniaturization associated with greater performance driven by a wide range of applications, such as stacked packages within mobile devices and other consumer products.

Today, most semiconductor wafers are thinned down to a range of 100 µm-200 µm especially when it comes to memory, CMOS Image Sensors (CIS) and power applications.

However, some silicon wafers are thinned down well below 100 µm in High Volume Manufacturing (HVM), including some 3D stacked memory devices, CIS and power devices. The total memory architecture thickness varies typically from 50 µm to 400 µm depending on the manufacturer and the packaging technology. For instance, standard memory, like DRAM or 2D NAND, uses silicon wafers that are thicker than 200 µm, while 3D stacked DRAM keeps moving downward, from 50 µm to 30 µm thick silicon substrates by 2025. Incidentally, the 30 µm to 50 µm thickness range is the one in which the largest number of thinned wafers is expected by 2025.

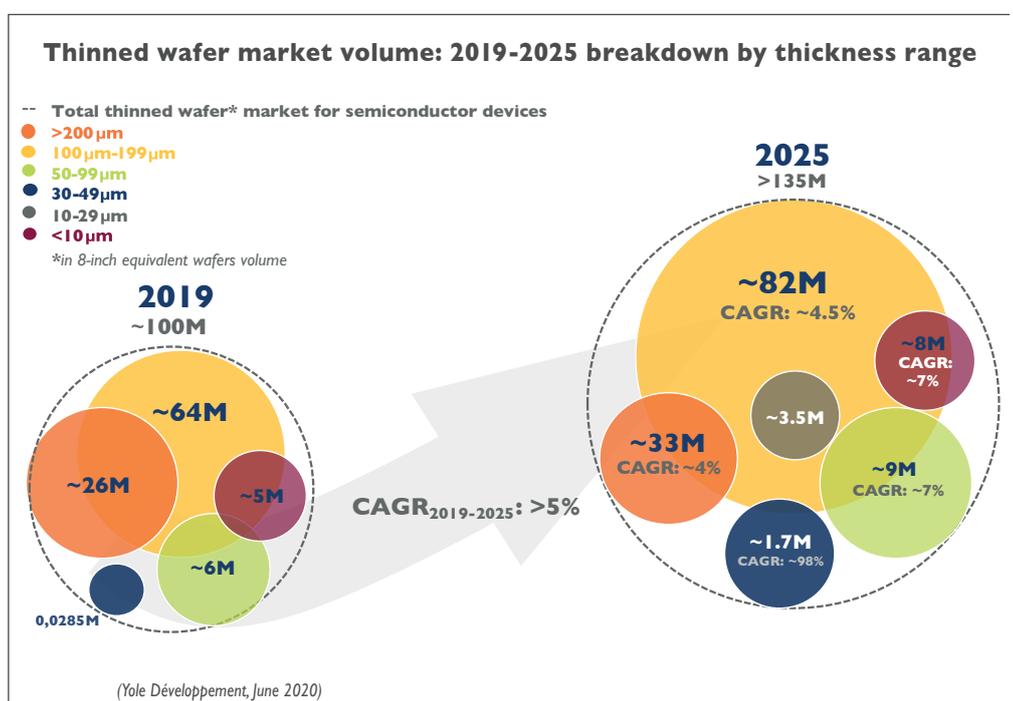
Meanwhile, Back-Side Illumination (BSI) CIS wafers are thinned down below 10 µm thickness

and are today the thinnest wafers across all semiconductor applications.

The thickness of power devices depends on applied voltage as well as semiconductor substrate type. From a wafer substrate point of view, Si-based MOSFETs involve wafer thickness of around 50 µm to 55 µm on 300 mm diameter wafers in HVM with a trend towards thinning down to 30 µm. Wafer thicknesses for SiC-based devices are rarely lower than 200 µm even though thickness reduction is expected to go down to 100 µm/110 µm in the next few years.

Typical wafer thickness for MEMS sensors is today in a range of 200 µm to 350 µm, especially for inertial MEMS. RF wafers devices are in the range of 140 µm and 200 µm and are opposite to every other the semiconductor devices in terms of thickness reduction. RF device wafers are getting thicker, with the thickness depending on whether wire bonding or flip-chip packaging will be more widely adopted by the industry.

Forecasts for the number of thinned wafers by thickness and by application are analyzed in this report.



ALTHOUGH THERE ARE COMMON DRIVERS, SOME OF THEM DIFFER DEPENDING ON THE SEMICONDUCTOR DEVICE

Myriad thinning technology steps are applied for the fabrication of semiconductor devices. At the back-end wafer stage, thinning methods are employed for thinning down the wafers and sometimes even removing the substrate, for LEDs on Si for example. Although there are similar and common drivers for thinning's applicability in semiconductor applications, the reasons for using such techniques differ from one device to another and depend on the end-applications. This is a critical point as it demonstrates that a change in architecture or a disruptive technology with potential large volumes involved can have a tremendous impact on the wafer thinning equipment market. The microLED market, should it take off and should it use backthinning technologies, could give a significant boost both to wafer-starts and to the corresponding equipment

market. The same can be said for CIS, 3D sensing applications or a widespread shift to System-in-Package (SiP) technology.

As of today and in the case of MEMS devices, such components are typically composed of a stack of a sensor element wafer, a cap and an Application Specific Integrated Circuit (ASIC). All three wafers must be thinned to reduce the size of the device.

With respect to power devices, thin wafers are needed here since reduced thickness lowers on-resistance, improves current carrying capability and minimizes power consumption.

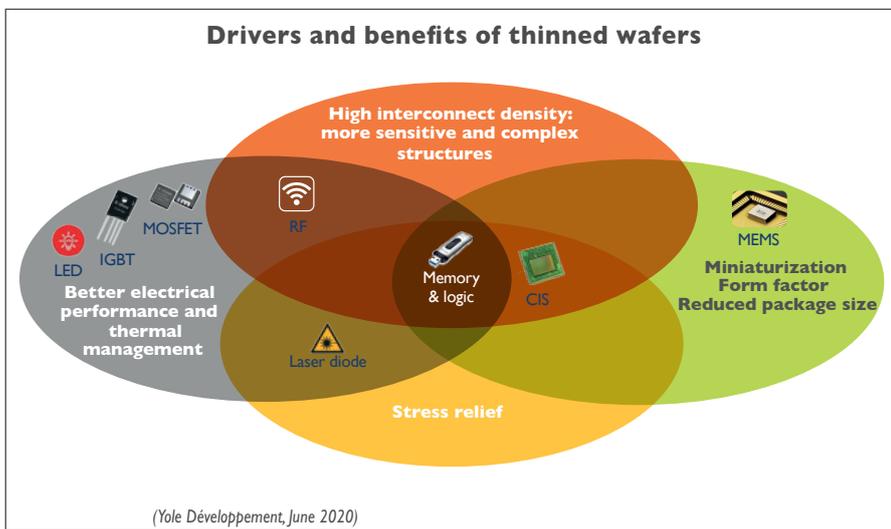
On the other hand, CMOS image sensor wafers are thinned down for TSV packaging where thinning is needed to achieve a very small form factor. BSI with extreme thinning below 10 µm enhances light sensitivity, while hybrid stack and triple stack architectures are pushing the boundaries further.

Traditional LED fabrication also requires a thinning or a removal step at the back-end for miniaturization and easier dicing/singulation.

Laser diode requirements are much less stringent but the emergence of high-power VCSELs demands much thinner wafers for enhanced heat management.

In the case of memory devices, further thickness reduction is driven by the need to maximize memory capacity of single packages, improved data transfer rates as well as power consumption mostly fueled by mobile applications.

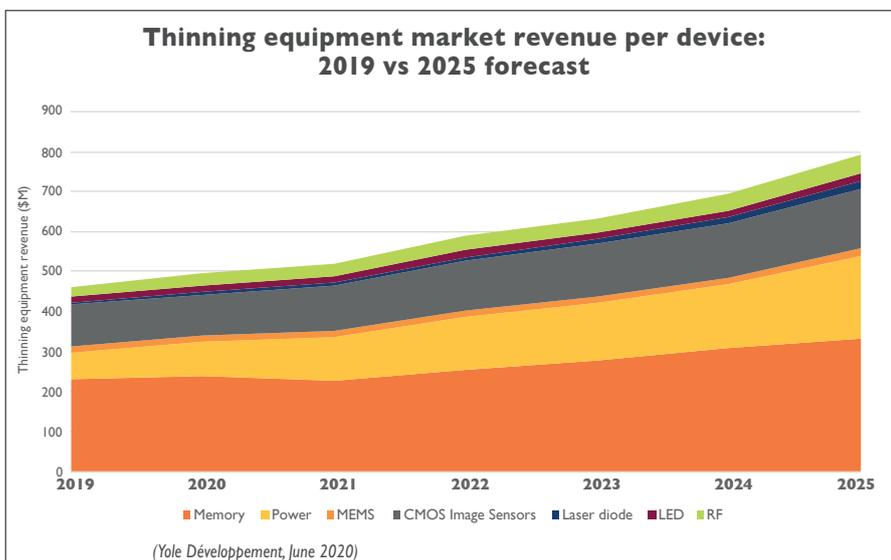
This report will present the key drivers for thinning down semiconductor wafers along with a detailed analysis by device.



COMPLEX SEMICONDUCTOR DEVICE ARCHITECTURES COUPLED WITH SMALL FORM FACTORS BRING NEW BUSINESS OPPORTUNITIES IN THE THINNING EQUIPMENT MARKET

The overall thinning equipment market was worth almost \$461M in 2019 and will exceed almost

\$792M by 2025 mainly generated by memory, CIS and power SiC components as well as LED and laser diodes.



Today, grinding is the most conventional thinning process used by semiconductor applications, reducing wafers from an average initial thickness of 750 µm to 400 µm.

Below 100 µm, wafers become mechanically flexible and challenging to handle, making further thinning down quite complex. Consequently, additional stringent thinning steps such as chemical-mechanical planarization (CMP) are required for some applications like CIS to obtain the best die quality possible.

When looking at the competitive landscape, the thinning equipment market is highly concentrated under the control of Japanese equipment vendors. Disco and Accretech hold more than 60% of the total thinning equipment business.

These companies have developed expertise in very specific back-end equipment lines where legacy equipment suppliers do not have the capabilities to support such processes. In addition, Disco and Accretech offer an impressive capability portfolio in terms of wafer processing equipment, from R&D to the most stringent manufacturing processes. The dominant Japanese players have been historically involved in the field for the past few decades. Disco is also licensing processes, such as the Taiko process that has already been adopted in mass production in power devices from key manufacturers like Infineon or STMicroelectronics for the backside metallization layer for 650V-1200V IGBTs and 40V-100V MOSFETs. This further concentrates the market.

Nonetheless, new players are also emerging. They tend to focus on a specific materials and/or applications. The complexity and the necessary know-how to develop low thickness processes open new business opportunities. As wafer backthinning is becoming increasingly widespread at the back-end substrate level, it leaves further business opportunities for other players to capture share in this sector. For example, Revasum is successfully focusing on thinning down non-Si based devices based on materials like SiC. Ebara is an example of a company focusing on one specific application, on memory in this instance.

The report quantifies the thinning equipment market in revenue and number of tools, broken down by semiconductor applications as well as the market share of the major thinning equipment vendors.

COMPANIES CITED IN THE REPORT (non exhaustive list)

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Bank code: 30056
Branch code: 00170
Account n°: 0170 200 1565 87
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