Thinning Equipment Technology and Market Trends for Semiconductor Devices

Market and Technology Report 2020
The main objectives of this report are as follows:

- To identify and describe which wafers can be classified as "thinned wafers".
- To update the business status of the markets for wafer thinning and thinning equipment & materials technologies.
- To analyze the key market drivers, benefits, and challenges of thinning technologies, by application.
- To describe the different existing technologies, their trends and roadmaps.
- To analyze the supply chain and technologies landscape for thinning equipment & materials.
- To provide a market forecast for thinning equipment & materials in the coming years, and an estimate of future trends.

The thinning markets are studied from the following angles:

- State-of-the-art technologies and trends
- Applications and drivers of thinning technologies
- Market value in terms of equipment and materials
- Industrial supply chain & value chain
Yole’s market forecast model is based on the matching of several sources:

**Comparison with existing data**
- Monitoring of corporate communication
- Using other market research data
- Yole analysis (consensus or not)

**Comparison with prior Yole reports**
- Recursive improvement of dataset
- Customer feedback

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**Top-to-bottom approach**
- Aggregate of market forecasts @ System level

**Bottom-up approach**
- Ecosystem analysis
- Aggregate of all players’ revenue @ System level

**Preexisting information**

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**Market**
- Volume (in Munits)
- ASP (in $)
- Revenue (in $M)

**Top-to-bottom approach**
- Aggregate of market forecast @ Semiconductor device level

**Bottom-up approach**
- Ecosystem analysis
- Aggregate of key players’ revenues @ Semiconductor device level

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**Secondary data**
- Press releases
- Industry organization reports
- Conferences

**Primary data**
- Reverse costing
- Patent analysis
- Annual reports
- Direct interviews

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**Information Aggregation**

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**Semiconductor foundry activity**
- Capacity investments and equipment needs
Amandine PIZZAGALLI

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Gaël Giusti, PhD. Is a Technology & Market Analyst specialized in Semiconductor Manufacturing as well as Equipment & Materials at Yole Développement (Yole). As part of Yole’s Semiconductor & Software division, Gaël’s expertise is focused on thin film growth and related applications, equipment, materials, and manufacturing processes. He is daily involved in the production of technology & market reports and custom consulting projects. Prior to Yole, Gaël served as an R&D engineer at Sil’Tronix Silicon Technologies for five years, in charge of upscaling a CVD process to develop epitaxial AlN thin film on sapphire for RF applications. He also worked on transparent conducting thin films for optoelectronics applications as a post-doctoral researcher at LMGP (Grenoble, France). Gaël holds a master’s degree from ENSICAEN (Caen, France) as well as a PhD in Materials Science from the University of Birmingham (UK).

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COMPANIES CITED IN THIS REPORT

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THINNING TECHNOLOGIES: FEATURES CAPABILITIES

Architecture

(Double Side) Lapping

Coarse Grinding
Fine Grinding

(CMP) polishing

Wet etching
Dry etching

Mechanical flexibility

Thinning Technologies

Dies/Devices

Thin films

Thin wafers
Si, SiC, GaAs, InP, LiTaO₃, LiNBO₃

Ultrathin wafers Si

Standard wafers
Si, Al₂O₃

Die Device

Thin film

Wafer

Thin films

Ultrathin wafers Si

Wet etching
Dry etching

Wafers/layer thickness

500 µm
350 µm
100 µm
50 µm
1 µm
0.5 µm
0.01 µm

TSV reveal

Report focus

APPLICATIONS REQUIRING THINNING PROCESS

Memory
- Laser diode*
  - Edge emitting laser
  - VCSEL

LED
- Traditional, microLED, miniLED
- GaAs LED based devices (IR LED, ROY LED)
- GaN LED based devices (UV LED, blue/green LED)

RF
- Power amplifiers, antenna switches

Power
- MOSFET
- IGBT
- Bipolar

MEMS detectors/Actuators

CMOS Image Sensors
### Thinning Processes Applied in the Semiconductor Field

**From front-end to back-end assembly**

<table>
<thead>
<tr>
<th>PROCESSING</th>
<th>PROCESS STEP LEVEL</th>
<th>ROLE</th>
<th>EQUIPMENT TECHNOLOGY</th>
<th>MATERIAL FUNCTION</th>
<th>APPLICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Removal process</td>
<td>Post-slicing after ingot growth</td>
<td>Thinning</td>
<td>Thickness reduction</td>
<td>Grinding, Lapping</td>
<td>All semiconductor applications</td>
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<tr>
<td></td>
<td></td>
<td>Planarization</td>
<td>Stress reduction, Defect-free surface</td>
<td>Lapping, CMP</td>
<td></td>
</tr>
<tr>
<td>Layer/Film level</td>
<td>Planarization to remove topography</td>
<td>Planarization</td>
<td>Smooth and planar surface</td>
<td>CMP</td>
<td></td>
</tr>
<tr>
<td>Wafer substrate</td>
<td></td>
<td></td>
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<td></td>
<td>Memory &amp; logic, Power HEMT</td>
</tr>
<tr>
<td></td>
<td>Thinning</td>
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<tr>
<td></td>
<td></td>
<td>Miniaturization</td>
<td>Grinding, CMP, Dry</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Electrical performances</td>
<td>Grinding, TAIKO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**MATERIAL FUNCTION**
- **Metal Cu, W, Al**
- **Dielectric (Oxide, Polymer)**
- **Silicon**, **SiC**, **Sapphire**, **GaAs**, **Glass**

**APPLICATIONS**
- Memory & logic
- Power HEMT
- Memory, MEMS, Laser diode, RF, CIS
THINNED WAFERS - DRIVERS AND BENEFITS

- High interconnect density: more sensitive and complex structures
  - Memory & logic
  - Stress relief

- Better electrical performance and thermal management
  - LED
  - IGBT
  - MOSFET
  - Laser diode

- Miniaturization
  - Form factor
  - Reduced package size
  - MEMS
## THINNING DRIVERS BY DEVICE

<table>
<thead>
<tr>
<th></th>
<th>Miniaturization, 3D stacking</th>
<th>Thermal management</th>
<th>Higher performance</th>
<th>“Hard” physical limitations</th>
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</thead>
<tbody>
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<td><strong>Memory and logic</strong></td>
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<td>![Checkmark]</td>
<td>![Checkmark]</td>
<td>Mechanical support Handling*</td>
</tr>
<tr>
<td><strong>CIS</strong></td>
<td>![Checkmark]</td>
<td>![Checkmark]</td>
<td>![Checkmark]</td>
<td>Mechanical support Handling*</td>
</tr>
<tr>
<td><strong>MEMS</strong></td>
<td>![Checkmark]</td>
<td></td>
<td></td>
<td>Mechanical deformation for wafers &lt; 100 µm</td>
</tr>
<tr>
<td><strong>RF</strong></td>
<td></td>
<td>![Checkmark]</td>
<td></td>
<td>Substrate dielectric loss</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td></td>
<td>![Checkmark]</td>
<td>![Checkmark] (reduced power consumption)</td>
<td>Substrate dielectric breakdown</td>
</tr>
<tr>
<td><strong>LED (excluding microLED)</strong></td>
<td></td>
<td>![Checkmark]</td>
<td>![Checkmark] (enhanced light extraction)</td>
<td>Mechanical support Handling*</td>
</tr>
<tr>
<td><strong>Laser diode</strong></td>
<td></td>
<td>![Checkmark]</td>
<td>![Checkmark] (for high-power)</td>
<td>Mechanical support Handling*</td>
</tr>
</tbody>
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*Wafer handling during the manufacturing and assembling processes, ESD related issues.
WAFER THINNING TRENDS
2019 vs 2025

<table>
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<tr>
<th>TODAY (2019)</th>
<th>TOMORROW (2025)</th>
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<tbody>
<tr>
<td>MEMS substrates</td>
<td>370–250 µ</td>
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<tr>
<td>MEMS capping</td>
<td>100–300µ</td>
</tr>
<tr>
<td>ASIC MEMS</td>
<td>100–150µ</td>
</tr>
<tr>
<td>CIS Packaging</td>
<td>140–200µ</td>
</tr>
<tr>
<td>CIS BSI</td>
<td>&lt;10 µ (3–5µ)</td>
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<tr>
<td>Memories</td>
<td>50 µm</td>
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<tr>
<td>Logic</td>
<td>50µ</td>
</tr>
<tr>
<td>Power Devices</td>
<td>60–110µ (depending on the voltage applied)</td>
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<tr>
<td>RF Devices</td>
<td>130µ</td>
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<tr>
<td>LEDs</td>
<td>100µ</td>
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<tr>
<td>Laser diode</td>
<td>100µ</td>
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</table>

In general, the thinning trends are down. The magnitude of these downturns depends on the maturity of the technology and on the substrate material used. There is a noticeable exception for power applications whereby a particular packaging technology authorizes a thicker (than today’s conventional thicknesses) substrate to be used.

Transition wire-bond → flip-chip technology
# Thinning Wafer by Thickness Range

<table>
<thead>
<tr>
<th>Application</th>
<th>Si/Si</th>
<th>SiC/SiC</th>
<th>GaAs</th>
<th>GaN Active layer</th>
<th>InP</th>
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</thead>
<tbody>
<tr>
<td>Laser diode</td>
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<td>EELs</td>
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<td>VCSEL</td>
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<td>Laser</td>
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<td>Power</td>
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<td>MEMS</td>
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<td>CMOS Image Sensor</td>
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<td>MEMS</td>
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<tr>
<td>CMOS Image Sensor</td>
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**Lower volume**
TOTAL THINNED WAFER - BREAKDOWN BY THICKNESS RANGE (8-INCH EQUIVALENT)

Total Thinned wafer - Breakdown by Thickness range (8-inch equivalent) for Semiconductor devices

- >200 µm
- 100 µm - 199 µm
- 50-99 µm
- 30-49 µm
- 10-29 µm
- <10 µm

* in 8-inch equivalent wafers volume

2019
~100M

~64M
~26M
~6M
~5M

CAGR<sub>2019-2025</sub>: ~>5%

2025
>135M

~ 82M
CAGR: ~+4.5%

~33M
CAGR: ~+4%

~8M
CAGR: ~+7%

~3.5M
CAGR: ~+7%

~3.3M

~9M
CAGR: ~7%

~1.7M
CAGR: ~98%
THINNING PROCESSES VS. WAFER THICKNESS – GENERAL TRENDS

Thickness (µm)/Technology applied

750 µm

- MEMS

~120 µm

- Grinding limitations
- Power devices

50 µm

- CMP limitations
- Memory & Logic

CIS packaging

BSI CIS
THINNING TECHNOLOGIES REQUIRED FOR EACH APPLICATION

<table>
<thead>
<tr>
<th>Thinning technologies vs applications</th>
<th>Memory</th>
<th>MEMS</th>
<th>Power</th>
<th>CMOS Image Sensor</th>
<th>RF</th>
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<tr>
<td>Wet etching/Dry</td>
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<td>✔️</td>
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</table>

OVERALL THINNING EQUIPMENT MARKET IN REVENUE (2019 VS 2025)

Overall thinning equipment market for semiconductor devices (in Revenue)
Breakdown by semiconductor device

Thinning equipment revenue ($M)

- Memory
- Power
- MEMS
- CMOS Image Sensors
- Laser diode
- LED
- RF

2019 2020 2021 2022 2023 2024 2025
Applications requiring wafer thinning

**Key technical steps, drivers, limitations, roadmap and real-world examples (cross-sectional views)**

Applications covered:
- Memory
- MEMS
- Power
- CIS
- RF
- Lighting
- Laser diodes
MORE SLIDE EXTRACTS

Market shares

**2019 THINNING EQUIPMENT MARKET SHARE**
Split by equipment vendor

**GRINDING AND CMP: EQUIPMENT SUPPLIER OVERVIEW**

<table>
<thead>
<tr>
<th>Company name</th>
<th>Grinding</th>
<th>CMP</th>
<th>Cluster (grinding + CMP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>[Diagram]</td>
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<td>[Diagram]</td>
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<tr>
<td>CIS</td>
<td>[Diagram]</td>
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</table>

**THINNING/POLISHING EQUIPMENT MARKET SHARE SUMMARY IN 2019**

*Non-exhaustive list*

Market forecast as well as 2019 market share are included in this report.
Contact our Sales Team for more information.

YOLE GROUP OF COMPANIES RELATED REPORTS & MONITORS

Yole Développement

Epitaxy Growth Equipment for More Than Moore Devices Technology and Market Trends 2020

CMOS Image Sensor Quarterly Market Monitor

Compound Semiconductor Quarterly Market Monitor

NAND & DRAM Quarterly Market Monitors

Status of the MEMS Industry 2019
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