# TABLE OF CONTENTS

**Part 1/2**

- Table of contents 002
- Scope of report 004
- Report methodology & definitions 005
- About the author 006
- Yole Group of companies related reports 007
- Glossary 008
- Companies cited in this report 009
- What we got right, What we got wrong 010
- 3-Page summary 011
- Executive summary 015
- Context 073
  - Scope of Fan-Out packaging 074
  - Fan-Out packaging definition 077
  - Fan-Out packaging introduction 081
  - Fan-Out packaging process flow 085
  - Fan-Out packaging segmentation 093
- Market forecasts 102
  - Fan-Out packaging revenue forecasts 103
    - Total overview
    - End-market
    - Impact of COVID-19
    - Core FO vs HD FO vs UHD FO
    - FOWLP vs FOPLP
    - Breakdown by carrier type & market segment
    - Application
- Fan-Out packaging unit forecasts 114
  - Total overview
  - End-market
  - Production Volume, 300mm wafer equivalent
  - Core FO vs HD FO vs UHD FO
- Market shares 120
  - What’s New? 121
  - Market shares of manufacturers 123
  - Market shares of IC substrate vs Fan-Out technologies 129
  - Market shares of business models 133
    - Reason behind TSMC dominance 142
  - Chapter conclusion 142
- Supply Chain 144
  - What’s New? 145
  - Supply chain overview 147
  - Global mapping 152
  - Fan-Out key suppliers activity summary 155
  - Analysis of the latest developments in supply chain 162
  - Apple and TSMC contract expires by 2021: What to expect? 168
  - Deca’s new business model 173
  - Nepes’ new fan-out packaging company spin-off: nepes laweh 175
  - Introduction of new players in Fan-Out packaging 180
  - Chapter conclusion 185

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TABLE OF CONTENTS

Part 2/2

- **Market trends**
  - Market drivers
  - Mobile AiP is trending with 5G
  - Why is Fan-Out packaging being adopted in AiP?
  - Big Die packaging is trending in HPCs
  - Why is Fan-Out packaging being adopted for HPC?
  - Fan-Out packaging in automotive radar
  - Why is Fan-Out packaging being adopted in radar?
  - Fan-Out packaging drivers
  - Chapter conclusion

- **Commercialization status**
  - What’s new?
  - Overview
  - Commercialization window by I/O Count & package size
  - PMIC
  - Audio codec
  - Automotive radar
  - Smartphones: APE
  - Mobile: AiP
  - Smartwatches
  - HPC
  - Chapter conclusion

- **Technology Trends**
  - What’s New?
  - Fan-Out packaging technology roadmaps
  - Fan-Out packaging technology by manufacturers
  - Fan-Out packaging technical challenges
  - Perspective on technology
  - Chapter conclusion

- **Fan-Out panel level packaging**
  - Panel-trends and motivation
  - FOPLP supply chain
  - Global map of FOPLP manufacturers
  - FOPLP supplier status
  - FOWLP vs FOPLP penetration rate
  - Reality of panel penetration
  - Chapter conclusion

- **Report conclusion**
- **Appendix**
- **Yole Développement corporate presentation**
Favier Shoo

Favier Shoo is a Technology and Market Analyst in the Semiconductor & Software division at Yole Développement, part of Yole Group of Companies. Based in Singapore, Favier is engaged in the development of technology & market reports as well as the production of custom consulting reports.

During 7 years at Applied Materials as a Customer-Application-Technologist in the advanced packaging marketspace, Favier developed a deep understanding of the supply chain and core business values. As an acknowledged expert in this field, Favier has provided training and held numerous technical review sessions with industry players. In addition, he has obtained 2 patents.

Prior to that, Favier worked at REC Solar as a Manufacturing Engineer to maximize production capacity.

Favier holds a Bachelor in Materials Engineering (Hons) and a Minor in Entrepreneurship from Nanyang Technological University (NTU) (Singapore). Favier was also the co-founder of a startup company where he formulated business goals, revenue models and marketing plans.

Contact: favier.shoo@yole.fr
COMPANIES CITED IN THIS REPORT

The main objectives of this report are:

• To identify and describe which technologies can be classified as ‘Fan-Out Packaging’
• To define clearly the different market classes of Fan-Out Packaging
• To analyze key market drivers, benefits and challenges of Fan-Out Packages by application
• To describe the different existing technologies, their trends and roadmaps
• To analyze the supply chain and Fan-Out landscape
• To update the business status of Fan-Out technology markets
• To provide a market forecast for the coming years, and estimate future trends

Fan-Out Packaging markets are studied from the following angles:

• Top-down based on end-systems demand
• Market valuations based on top-down and bottom-up models
• Market shares based on production projections
• Supply value chain analysis
• State-of-the-art technologies and trends
• End-user application adoptions
Yole’s market forecast model is based on the matching of several sources:

Comparison with existing data
- Monitoring of corporate communication
- Using other market research data
- Yole’s analysis (consensus or not)

Comparison with prior Yole reports
- Recursive improvement of dataset
- Customer feedback

- Top-down approach
  - Aggregate of market forecasts
    @ System level

- Top-down approach
  - Aggregate of market forecasts
    @ Semiconductor device level

- Bottom-up approach
  - Ecosystem analysis
    @ System level
  - Aggregate of all players’ revenues

- Bottom-up approach
  - Ecosystem analysis
    @ Semiconductor device level
  - Aggregate of key players’ revenues

- Information Aggregation

Primary data
- Reverse costing
- Patent analysis
- Annual reports
- Direct interviews

Secondary data
- Press releases
- Industry organization reports
- Conferences

**REPORT METHODOLOGY & DEFINITIONS**
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Meaning</th>
</tr>
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<tbody>
<tr>
<td>ADAS</td>
<td>Advanced Driver-Assistance Systems</td>
</tr>
<tr>
<td>AiP</td>
<td>Antenna in Package</td>
</tr>
<tr>
<td>APE</td>
<td>Application Processor Engine</td>
</tr>
<tr>
<td>APU</td>
<td>Application Processor Unit</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application-Specific Integrated Circuit</td>
</tr>
<tr>
<td>BEOL</td>
<td>Back-end Of Line</td>
</tr>
<tr>
<td>BGA</td>
<td>Ball Grid Array</td>
</tr>
<tr>
<td>BOM</td>
<td>Bill Of Materials</td>
</tr>
<tr>
<td>CAGR</td>
<td>Compound Annual Growth Rate</td>
</tr>
<tr>
<td>CSP</td>
<td>Chip Scale Package</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>DTOR</td>
<td>Development Tool of Record</td>
</tr>
<tr>
<td>ECD</td>
<td>Electro-Chemical Deposition</td>
</tr>
<tr>
<td>EMC</td>
<td>Epoxy Mold Compound</td>
</tr>
<tr>
<td>ePLP</td>
<td>embedded Package-Level-Packaging</td>
</tr>
<tr>
<td>ePoP</td>
<td>embedded Package-on-Package</td>
</tr>
<tr>
<td>eWLB</td>
<td>embedded Wafer-Level BGA</td>
</tr>
<tr>
<td>F2F</td>
<td>Face-to-Face</td>
</tr>
<tr>
<td>FC</td>
<td>Flip-Chip</td>
</tr>
<tr>
<td>FO</td>
<td>Fan-Out</td>
</tr>
<tr>
<td>FOPLP</td>
<td>Fan-Out Panel-Level Packaging</td>
</tr>
<tr>
<td>FOWLP</td>
<td>Fan-Out Wafer-level Packaging</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field-Programmable Gate Array</td>
</tr>
<tr>
<td>HBM</td>
<td>High Bandwidth Memory</td>
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<tr>
<td>HD FO</td>
<td>High Density Fan-Out</td>
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<tr>
<td>HDI</td>
<td>High Density Interconnect</td>
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<tr>
<td>HPC</td>
<td>High Performance Computing</td>
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<tr>
<td>HVM</td>
<td>High-Volume Manufacturing</td>
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<tr>
<td>I/O</td>
<td>Inputs/Outputs</td>
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<tr>
<td>IC</td>
<td>Integrated Circuits</td>
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<tr>
<td>IDM</td>
<td>Integrated Device Manufacturers</td>
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<tr>
<td>inFO</td>
<td>integrated Fan-Out</td>
</tr>
<tr>
<td>IP</td>
<td>Intellectual Property</td>
</tr>
<tr>
<td>IPD</td>
<td>Integrated Passive Devices</td>
</tr>
<tr>
<td>L/S</td>
<td>Line/Space</td>
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<tr>
<td>LiDAR</td>
<td>Light Detection and Ranging</td>
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<tr>
<td>LTE</td>
<td>Long-Term Evolution</td>
</tr>
<tr>
<td>LVM</td>
<td>Low Volume Manufacturing</td>
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<tr>
<td>MCM</td>
<td>Multi-Chip Module</td>
</tr>
<tr>
<td>MCP</td>
<td>Multi-Chip Package</td>
</tr>
<tr>
<td>MEMS</td>
<td>Micro-Electro-Mechanical System</td>
</tr>
<tr>
<td>mmWave</td>
<td>Millimeter wave</td>
</tr>
<tr>
<td>NR</td>
<td>New Radio</td>
</tr>
<tr>
<td>OEM</td>
<td>Original Equipment Manufacturer</td>
</tr>
<tr>
<td>OSAT</td>
<td>Outsource Semiconductor Assembly and Test</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PDN</td>
<td>Power Distribution Network</td>
</tr>
<tr>
<td>PMIC</td>
<td>Power Management Integrated Circuit</td>
</tr>
<tr>
<td>PMU</td>
<td>Power Management Unit</td>
</tr>
<tr>
<td>PoP</td>
<td>Package-on-Package</td>
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<tr>
<td>PTOR</td>
<td>Production Tool of Package</td>
</tr>
<tr>
<td>PVD</td>
<td>Physical Vapor Deposition</td>
</tr>
<tr>
<td>PWB</td>
<td>Printed Wiring Board</td>
</tr>
<tr>
<td>QFN</td>
<td>Quad-Flat No-Lead Package</td>
</tr>
<tr>
<td>Radar</td>
<td>RAdio Detection And Ranging</td>
</tr>
<tr>
<td>RCC</td>
<td>Resin Coated Copper</td>
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<tr>
<td>RCP</td>
<td>Redistributed Chip Package</td>
</tr>
<tr>
<td>RDL</td>
<td>Redistribution Layer</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>SiP</td>
<td>System-in-Package</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-Chip</td>
</tr>
<tr>
<td>TMV</td>
<td>Through-Mold-Via</td>
</tr>
<tr>
<td>TPV</td>
<td>Through-Package-Via</td>
</tr>
<tr>
<td>TSV</td>
<td>Through-Silicon-Via</td>
</tr>
<tr>
<td>TTV</td>
<td>Total Thickness Variation</td>
</tr>
<tr>
<td>UBM</td>
<td>Under Bump Metallization</td>
</tr>
<tr>
<td>UHD FO</td>
<td>Ultra-High-Density Fan-Out</td>
</tr>
<tr>
<td>WL CSP</td>
<td>Wafer-Level Chip-Scale Package</td>
</tr>
<tr>
<td>WL FO</td>
<td>Wafer-Level Fan-Out</td>
</tr>
</tbody>
</table>
EMBEDDED PACKAGING TECHNOLOGIES

Embedded packaging technologies with connections fanned out of IC surface

Fan-Out Packaging (Focus of the report)

Embedded Die

Embedding in organic laminate

- Lamination around the chip
- Cavity dug in substrate

Encapsulator type

- CF / CL
- CL

Process type

- RDL
- Foundry BEOL + RDL

Interconnection type

- FU / FD

Chip placing

- Chip-First: CF
- Chip-Last: CL
- Face-Up: FU
- Face-Down: FD

Chip orientation

- FU / FD

Advanced Substrate

Flip-Chip

Chip orientation

- FU / FD

Chip placing

- CF / CL

Interconnection type

- RDL

Process type

- Foundry BEOL + RDL

Encapsulator type

- CF / CL

Embedding in epoxy mold compound
Fan-Out Packaging can be understood in several ways depending on who we are talking to. It is especially confusing because when the hype around this package type began, many players used the name ‘Fan-Out’ to describe their solution to gain more attention in the market.

An even more confusing aspect is that acknowledged Fan-Out solutions are not, or were not, called ‘Fan-Out’ by their creators. For instance, Infineon, creator of eWLB, one of the most widespread Fan-Out solutions, had not even called it ‘Fan-Out’ in its IP and referred to it for a long time as an ‘embedded die’ solution.

An acknowledged characteristic of ‘Fan-Out’ packages is that, as the name suggests, interconnections are fanned out on the chip and because of that, bumping is not dependent on die surface.

This means that Fan-Out has the potential to achieve any number of interconnects with standard pitches at any shrink stage of the wafer node technology.

If the only definition of ‘Fan-Out’ is a package from which connections and bumping are out of the chip scale, then almost all packages can be defined as Fan-Out. Flip-Chip BGA, Flip-Chip CSP, Embedded Die, etc. Due to this, confusion is high in the industry.

To make a fair comparison and to clarify the situation, Yole focuses on selected Fan-Out technologies that have at least one of these 2 key characteristics:

- Fan-Out solutions that use mold compound to embed the dies—not laminated materials.
- Fan-Out solutions that do not use IC substrates (PCB type of interposers) to fan out of chip area.
FAN-OUT PACKAGING DEFINITION BY MARKET CLASS

Core FO vs HD FO vs UHD FO

Core FO: Core Fan-Out
HD FO: High-Density Fan-Out
UHD FO: Ultra-High-Density Fan-Out

Core FO
- RF, PMU, BB, AiP etc.
- \( I/O \text{ per mm}^2 < 6 \)
- \( \text{RDL L/S} > 15/15\mu m \)

HD FO
- Mobile APE, AiP etc.
- \( 6 < I/O \text{ per mm}^2 < 12 \)
- \( 15/15\mu m > \text{RDL L/S} > 5/5\mu m \)

UHD FO
- Networking, servers etc.
- \( I/O \text{ per mm}^2 >> 18 \)
- \( \text{RDL L/S} << 5/5\mu m \)

In 2020 report, HD FO and UHD FO will be classified separately in order to be forward looking for market forecast due to the emergence of UHD FO.
FAN-OUT INTRODUCTION

Filling the I/O gap between IC and PCB evolution

Currently, FC-CSP/FC-BGA are the most standard packages competing with fan-out. However, their cost is increasing fast with I/O density, mainly due to advanced substrate cost.

Fan-in WLCSP, fan-out’s main challenger, has earned large market share in the past five years due to its advantages (low cost, thin package). It is substrate-less, but faces inherent limitations due to available die area for re-routing.

Though both packages are struggling to fill the gap between ICs and PCBs, their evolutions are asynchronous. ICs have followed Moore’s law throughout their history and experienced size decreases much faster than PCBs, creating a mismatch.

Fan-out can have a number of interconnects with standard pitches independent of chip size, while also allowing multi-chip and 3D packaging solutions. This kind of flexibility can fill the gap between ICs and PCBs.
FAN-OUT PACKAGING PROCESS PRINCIPLE

01 Tape lamination

02 Pick and place

03 Wafer-level molding

04 Carrier removal (de-bonding)

05 Standard WLP process (Passivation, pattern, RDL, bonding)

06 Dicing

Fan-Out: Dies embedded in mold compound. No advanced substrate needed to fan out of chip surface.
eWLB example (chip-first face-down)

Source: Infineon
FAN-OUT PACKAGING REVENUE FORECASTS

FAN-OUT PACKAGING: REVENUE FORECAST

Revenue from FO : Split by End-Market

Fan-Out Packaging Market Revenue ($M)

By End-Market

$1,500M
$1,000M
$500M
$100M
$0

- Medical
- Telecommunications & Infrastructure
- Automotive & Mobility
- Mobile & Consumer
- Total

Within Fan-Out Packaging, Mobile & Consumer market dominates with revenue of $1,250M in 2019 projected to reach $1,498M at 12.5% CAGR. Mobile & Consumer and Telecom & Infrastructure end-markets influence the overall trend of Fan-Out Packaging.

In 2020, the world is experiencing an unprecedented pandemic, as the novel coronavirus, COVID-19 spreads rapidly on a global scale. The number of infected cases continues to increase in H1-2020 which has triggered a lockdown of countries one after another. This has caused a pandemic-driven contraction of economies, actively negatively impacting semiconductor development and production.

Fan-Out Packaging market is heavily dependent on Mobile & Consumer and Telecom & Infrastructure end-market demand, with 9% exposure in those markets as of 2019. So, it is inevitable for Fan-Out Packaging to experience a downturn in its market value in 2020, reflecting COVID-19 impact.

However, business is expected to bounce back fast in 2021. In fact, a massive upsurge in the demand in Telecom & Infrastructure is expected as end-users are not only coming to recognize the crucial role of technology (from supporting remote working to scaling digital operations due to lockdowns) but will also invest in and utilize it even more. Hence, end-system demand will accelerate in 2021.

To sum up, pent-up demand may return as soon as H2-2020. There is a light at the end of the tunnel as more technology related business leaders are increasingly optimistic that businesses and consumers will return to a new normal by 2021. Fan-Out Packaging will unreasonably rise this year up in 2021.
FAN-OUT PACKAGING: REVENUE FORECAST

2019

- HD FO: $534M (43%)
- UHD FO: $504M (40%)
- Core FO: $218M (17%)

$1,256M

Total Fan-Out Market Value CAGR 2019-2025 = 15.9%

2025

- HD FO: $1,291M (42%)
- Core FO: $231M (8%)
- UHD FO: $1,523M (50%)

$3,046M

CAGR 15.8%
CAGR 20.2%
CAGR 1.0%
FAN-OUT PACKAGING REVENUE FORECASTS

FAN-OUT PACKAGING: REVENUE FORECAST
Breakdown by Carrier Type & Market Class

FAN-OUT PACKAGING: REVENUE FORECAST
Revenue from FO: FOWLP vs FOPLP

FAN-OUT PACKAGING: REVENUE FORECAST
KEY TRENDS

Fan-Out Packaging Market Revenue ($M) By Market Class

UHD FO CAGR 2019-2024 >20%
HD FO CAGR 2019-2024 >15%
CORE FO CAGR 2019-2024 >1%
FAN-OUT PACKAGING UNIT FORECASTS

In terms of production volume, both FOWLP and FOPLP are growing, though FOWLP has grown significantly quicker at 42.5% CAGR.

However, FOWLP volume will still be more.

Fan-Out Packaging, 300 mm wfr. eq. (kwsqy)
By Carrier Types
Fan-Out Packaging is expected to experience a sharp growth for RF AiP applications (driven by 5G) at a whopping 76% CAGR. For cost effective HPCs, exceptional growth is projected at 52% and 20% CAGR respectively for (x)PU + HBM and (x)PU die partitioning. Strong growth of 14% CAGR for connectivity is expected as well, especially Bluetooth (RF) + other functions like MEMs, PAs or switches.
FAN-OUT ACTIVITIES: GLOBAL MAP OF MAIN PLAYERS*

*Showing mainly HQ. Non-exhaustive list of players: Numerous companies have an interest in Fan-Out…

Non-exhaustive list of companies

Newly added companies/sites in 2020 report
What's new in 2020 report?
- Added inFO Technology
- Removed HQ to prevent confusion
- Included manufacturing sites of the same company with different technologies, where ever possible

Amkor U.S. and Deca U.S. are no longer listed since these sites are not manufacturing in US.

Non-exhaustive list of companies

- eWLB Technology
- RCP Technology
- M-series Technology
- InFO Technology
- Other Fan-Out technology manufacturers
How are the individual business models positioning themselves for Fan-Out Packaging?

**OSATs**
- eWLB pioneers to enter market and now leading it by volume within Core FO. Staying with FOWLP for Core FO.
- Position FOPLP to reduce cost. Focused on large-die size applications for future. Attracts fabless customers like Mediatek
- Running LVM and qualification lots for HD FO. Not focused on Core FO.
- Collaboration of OSATs & R&D institutes to assess FO capabilities.

**IDM**
- Samsung Electronics (previously through SEMCO) has commercialized FOPLP with APE/PMIC for galaxy watch (consumer).
- Main focus is to enable HD FO for Samsung’s internal smartphone and if possible secure FE + Packaging business for Apple’s APE which was lost to TSMC in 2015.
- Outsourced majority of its production to OSATs. Runs R&D and LVM within internal units. Focus is on automotive market.
- New Licensing Position taken by Deca : Technology transfer of M-Series and Adaptive Patterning to leading manufacturers.

**Foundry**
- Only supplier of APE FE + Packaging for Apple’s iPhones and smartwatches.
- Expecting TSMC to utilize inFO for 5G and HPC applications. Tapping into new pool of customers, such as Mediatek, Nephos, HiSilicon and Nvidia for Fan-Out Packaging.
- Collaborated with R&D institutes to assess FO capabilities.

**OEMs / Fabless / Licensing**
- Since 2019, Fabless has been qualifying Fan-Out Packaging for mega-trend driven applications (5G, HPC, IoT).
- Emergence of new players in IoT and AiP field in 2020. They have been running LVM qualification lots since 2019.
FAN-OUT PACKAGING LATEST DEVELOPMENTS IN SUPPLY CHAIN

Key summary of leaders within each business model

- **FO SUPPLIER**
  - Leading Foundry: New customers since 2019...
    - TSMC

- **EXISTING CUSTOMERS**
  - Non-exhaustive list of companies
    - Existing customers

- **NEW CUSTOMERS**
  - Leading IDM: More HD FO adoptions?
    - Samsung

- **SPECULATIVE CUSTOMERS**
  - Leading Licensor: New business model in 2020...
    - Deca Technologies

Non-exhaustive list of companies
APPLE AND TSMC CONTRACT IS SET TO EXPIRE BY 2021: WHAT TO EXPECT?

Overview of Samsung and TSMC’s battle for Apple’s APE business

**Timeline of iPhone APE Supplier Business**

APE Die Supplier

APE Package Supplier

TSMC won the APE FE die business from Samsung but not the packaging business.

TSMC successfully clinched FE + Packaging deal and displaced Samsung. Dominated ever since…

In 2016, TSMC HD FO Packaging is commercialized

- **2013**
  - iPhone 5 (A6)
  - Samsung

- **2014**
  - iPhone 5S (A7)
  - Samsung

- **2015**
  - iPhone 6 (A8)
  - Samsung

- **2016**
  - iPhone 6S (A9)
  - Samsung

- **2017**
  - iPhone 7 (A10)
  - TSMC

- **2018**
  - iPhone 8 & X (A11)
  - TSMC

- **2019**
  - iPhone XS & XR (A12)
  - TSMC

- **2020**
  - iPhone 11 (A13)
  - TSMC

- **2021**
  - iPhone 12 5G (A14)
  - TSMC

- **2022**
  - iPhone ??
  - ?

Samsung successfully gained back APE FE business with packaging support as incentive

Samsung dominated Apple's APE business

Expected
The Analyst’s Point of View (1/3)

**Why is the TSMC-APPLE contract expiring in 2021?**

It is understood that Apple’s contract for TSMC’s foundry and packaging production of APE is set to expire by 2021. Consequently, we believe this also means that after Q3-2021 the business of Apple APE is open, no longer tied to TSMC. Knowing the history of how TSMC displaced Samsung before, a huge battle is brewing between TSMC and Samsung to secure this new sweet deal with Apple for the APE.

**Is Samsung Electronics fighting to win back this business?**

Yes, Samsung Electronics is stepping up its game by strengthening the synergy between semiconductor and packaging. A strong indication is the acquisition of SEMCO FOPLP technologies. This is an attempt to expedite the yield and other technical breakthroughs for FE + Packaging solution for Apple. Equally important, Samsung Electronics has the same model as TSMC now. They are able to provide bundled APE FE + Packaging solution for Apple. The expiry of TSMC’s contract is a very good chance to grab market back from TSMC. Although Samsung adopted HD FO in its smartwatch with in-house FOPLP technology, it is understood that the cost is not low because of yield issues. Internally, Samsung is struggling to enable an HD FO APE within its own mobile. At the moment, it is not looking ideal, but Samsung has the resources and capability to make the breakthrough in due course. The question is whether Samsung can achieve it in the shortest time possible and come up with an attractive solution in 2020 because qualification needs to start before 2021. Samsung is powerful in smartphone components (especially display and memory). Moreover, Samsung is in control of many designs and devices. However, being an IDM, Samsung is a supplier of package, memory and logic who also competes at the same time with everyone. For example, the Competitor-Customer relationship with TSMC(Apple)/Qualcomm makes the business political relationship with Apple very tricky.

**Let’s revisit why TSMC won in the first place and what’s the situation now?**

TSMC succeeded because they positioned an APE die FE + Packaging bundle that matched up extremely well (if not better) than what Samsung could provide. TSMC is the leading chip manufacturer, and is also in a favorable position to gain more business due to the soured relationships between Apple and Samsung in the smartphone business. Moreover, in recent years, TSMC was committed to stay ahead of Samsung and Intel on front-end scaling even though progress is generally slowing down (defying Moore’s Law) and becoming extremely expensive to scale. At the moment, it is understood that Apple is still pleased with TSMC inFO_PoP technology though is still pressuring for lower cost. The relationship between Apple and TSMC is healthy.
Who are all the possible suppliers for Apple for 2021 APE Packaging business?

TSMC and Samsung.

What are speculated PROS/CONS of potential suppliers from Apple’s perspective?

<table>
<thead>
<tr>
<th>SUPPLIER</th>
<th>PROS for Apple</th>
<th>CONS for Apple</th>
<th>Possibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td></td>
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<tr>
<td>Samsung</td>
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</table>
APPLE AND TSMC CONTRACT IS SET TO EXPIRE BY 2021: WHAT TO EXPECT?
The Analyst’s Point of View (3/3)

What is Apple’s possible take at the moment?

Based on semiconductor trends, Apple knows well that foundry scaling is becoming too expensive and challenging. Advanced packaging is the way to go for integrated devices, edge computing, and 5G applications in mobile devices. In general, we are certain Apple is a strong believer of Fan-Out Packaging. To Apple, uFO is not only horizontal but also vertical; it provides them the flexibility to design dies for different suppliers, flexibility within the shortest possible time-to-market. In fact, Apple will likely adopt more Fan-Out Packaging for 5G iPhone that is set to be released in 2020. In a nutshell, to win Apple’s APE business in 2020 and beyond, a high-quality and cost-competitive Fan-Out Packaging solution is required.

Analyst’s Final Take: Apple will most probably sign a new deal with TSMC beyond 2021

To sum up, there is no perfect supplier for Apple in this competitive APE business. Apple is the market leader over many other smartphone OEs. APAC largely because of their innovation and determination to come up with new ideas that nobody else has thought of. So, it is not only cost but also a proven HD FO solution with scalability and reliability. Moving forward, Apple will stick with Fan-Out Packaging with heterogeneous combinations while at the same time pushing down the cost.

Lowering prices is one of the oldest and quickest strategies to gain a larger market share but this was what TSMC has done in 2015 to win Apple’s APE business. In fact, TSMC added differentiated value with a bundled deal of APAC + Packaging. Of course, Apple and Samsung being at loggerheads in mobile business is also a motivation for Apple to remove Samsung as APE supplier.

So, Samsung’s strategy becomes even more critical in order to have a firm grip on the competitive landscape as TSMC moves to a market share growth strategy with more uFO developments. Samsung is fighting hard with strategic decisions by commercializing HD FO in smartphones, buying back MEMS and adopting a similar model to TSMC. But is Samsung in time to demonstrate capability before 2021? Probably not. Apple is now heavily reliant on TSMC after years of engaging since 2013. There is no business political opposition and the relationship between TSMC and Apple is known to be very healthy. It will take Samsung a lot more than cost to beat TSMC at this moment.
In February 2020, Deca becomes an independent technology development & licensing company.

A decade of innovation is now opening to the industry for advanced electronic interconnect, including:

- M-Series™ fan-out structure, process, equipment & materials;
- Adaptive Patterning™ real-time design providing freedom from historic physical mask constraints;
- Technology roadmap to sub-micron Adaptive Patterning in partnership with leading direct write lithography and support equipment;
- Emerging heterogeneous integration and chiplet implementations of M-Series & Adaptive Patterning.

Deca’s business model now includes:

- Technology transfers to leading manufacturing companies (Foundries, OSATs, semiconductor companies);
- License agreements to over 90 issued and pending patents with associated know-how in M-Series and Adaptive Patterning;
- Adaptive Patterning design systems in partnership with leading EDA providers combined with proven high-volume real-time design in manufacturing.
NEPES’ NEW SPIN-OFF FOR FAN-OUT PACKAGING: NEPES LAWEH

The Analyst’s Point of View

Analyst’s opinion
“Nepes is making a bold move that matters…”

Nepes Revenue Target

<table>
<thead>
<tr>
<th></th>
<th>2018</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nepes Group Revenue</td>
<td>~$330M</td>
<td>~$330M</td>
</tr>
<tr>
<td>Nepes Laweh Revenue</td>
<td>~$330M</td>
<td>~$330M</td>
</tr>
</tbody>
</table>

*Yole internal data calculation is $246M for Nepes group 2018 Revenue

Source: Korean and Chinese media news

Facts gathered from news & interviews

1. Nepes Laweh is engaged in the POWF and Launches its unit from China in January 2019 and is targeting to reach $1B in 2022 revenue.
2. The company reported 2017 revenue to local media of 12M (Korea) and 2.3B (China), around $200M.
3. Nepes Laweh claims to be taking business from module makers, and the 12M from China is for 2018, and the 2.3B is for 2019.
4. Nepes Laweh claims to be taking business from module makers, and the 12M from China is for 2018, and the 2.3B is for 2019.
5. Nepes Laweh claims to be taking business from module makers, and the 12M from China is for 2018, and the 2.3B is for 2019.
6. Nepes Laweh claims to be taking business from module makers, and the 12M from China is for 2018, and the 2.3B is for 2019.
7. Nepes Laweh claims to be taking business from module makers, and the 12M from China is for 2018, and the 2.3B is for 2019.
8. Nepes Laweh claims to be taking business from module makers, and the 12M from China is for 2018, and the 2.3B is for 2019.
FOPLP

The advanced packaging and testing business mainly includes three types of business: chip back-end packaging and testing, COF tape and reel, panel-level integrated packaging and testing.

ESWIN understands the development trend of More than Moore semiconductor devices toward miniaturization, high integration, and system integration. Among many advanced packaging technologies, ESWIN believes Fan-Out Packaging has many unique technical advantages. In the industry, the main pain point of Fan-Out Packaging is the high production cost on 300mm wafers, especially for large-size chips/systems. So, FOPLP technology uses a square carrier board, which has a large carrier board size, high utilization rate, high output rate, and less BOM waste. It can realize large-size chip/system integration and is the main low-cost research and layout direction of the industry.

Moreover, ESWIN has more than 20 years of established high-precision and large-screen technology as well as glass processing experience. This is integrated with mature semiconductor packaging technology to form FOPLP core technology with ESWIN’s independent intellectual property rights. Therefore, ESWIN is positioning itself to provide customers with high efficiency, performance and low-cost technical solutions and services.
FAN-OUT PACKAGING MARKET DRIVERS

* From 2020 onwards, market drivers are hypothesized based on interviews with industry players.
WHY IS FAN-OUT PACKAGING TRENDING FOR NEW APPLICATIONS?

WHY IS FAN-OUT PACKAGING TRENDING IN HPCS?

Fan-Out's role in this?

Reducing single unit die size helps to increase gross die and improve the yield. Industry players recognize this, and they are starting to split large dies into two or even four smaller dies for processing in order to resolve the yield loss and maintain the same bandwidth by means of advanced packaging. As interconnections between multi-chips substrate technology is necessary.

However, it becomes a great challenge in cost. Moreover, the resulting reliability high/low temperature and humidity cannot have been actively qualifying high-end showed Fan-Out Packaging can handle. Packaging can indeed increase the great, usually enormous and suffers low yield (MUST-in-MUST) is targeting 3DIC stacking computing.

Lastly, Fan-Out Packaging’s relative cost cheaper alternative. Eventually, Fan-Out Packaging for many applications. So Fan-Out Packaging’s role in this.
FAN-OUT PACKAGING KEY APPLICATIONS

**END-MARKET**

<table>
<thead>
<tr>
<th>Applications</th>
<th>Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Smartphones</td>
<td>APE</td>
</tr>
<tr>
<td></td>
<td>PMIC</td>
</tr>
<tr>
<td></td>
<td>Audio Codec</td>
</tr>
<tr>
<td></td>
<td>RF Transceivers</td>
</tr>
<tr>
<td></td>
<td>Baseband</td>
</tr>
<tr>
<td></td>
<td>RF Chip + AiP</td>
</tr>
<tr>
<td></td>
<td>APE + PMIC</td>
</tr>
<tr>
<td>Smartwatches</td>
<td>APE + Si Die</td>
</tr>
<tr>
<td>Headphones</td>
<td>MCU + BT</td>
</tr>
<tr>
<td>IoT Devices</td>
<td>Audio Codec + PMIC</td>
</tr>
<tr>
<td>HPCs</td>
<td>APE + NOR + PMIC</td>
</tr>
<tr>
<td></td>
<td>Networking, Cloud and AI chips</td>
</tr>
<tr>
<td></td>
<td>MMIC</td>
</tr>
<tr>
<td></td>
<td>MMIC + AiP</td>
</tr>
<tr>
<td>Handheld Portable</td>
<td>Ultrasound</td>
</tr>
</tbody>
</table>

*Non-exhaustive list of companies and products
New: Newly covered in this year’s report*
The Autus R10 tightly integrated CMOS design is optimized for performance and cost; including embedded RF and baseband processing, and 1T1R via integrated Antenna in Package. A simple, three wire interface is all that’s required to link to an external ECU. Mediatek positions this Radar Chipset as a compact, cost-performance optimized Ultra-Short-Range Radar (USRR) Platform. This Radar Chipset is found in Steelmate BSE151 System.
SMARTPHONE 5G MMWAVE AiP

Taking a peep into the future..

It is our understanding that there are no commercialized smartphone AiP products in H1-2020 - they would have to be 5G mmWave smartphones, not 5G Sub-6 smartphones. The earliest possible 5G mmWave smartphone available for teardown will be Apple’s 5G mmWave iPhone which is expected to be released in H2-2020. Knowing it is potentially packaged with Fan-Out Packaging, TSMC’s InFO_AiP will be focused here.

RF architecture is evolving to accommodate high performance computing’s power and footprint requirements. TSMC InFO covers the most comprehensive RF technology offering, covering sub-6GHz to mmWave to RF Front-end SOI applications.

For 5G mmWave wireless communication, InFO_AiP integrates dipole and patch antenna with mmWave FEM chip leveraging high density RDL and fine pitch. TSMC’s proprietary low-Dk dielectric material and uniform RDL enable high gain and low loss. TSMC has qualified InFO_AiP with a package dimension of 12mm x 12mm x 0.9mm with 2 RDL layers.

---

**RF Architecture for 5G mmWave AiP**

Source: TSMC

**TSMC InFO positioned for 5G mmWave AiP**

Source: TSMC
FAN-OUT IS SEEING ADOPTION IN SMARTWATCHES

Fitbit Charge 3: Fan-Out Packaging of Microcontroller + Bluetooth

Fitbit Charge 3

Bottom view

XRAY view

Die 2
Cypress Bluetooth Low Energy (BLE) SoC

Packaged by JCET (OSAT)

Die 1
Cypress MCU, Touch Controller

With Fitbit’s Charge 3, Cypress has combined two dies of different functionality into one microcontroller with Bluetooth. This process is thought to be packaged by JCET Group ( Ober-Chapel’s Singapore lab).

Die 1 - MCU is a Capacitive touch sensor technology which measures changes in the capacitance between a die and its environment in order to detect the presence of a finger on or near a touch surface.

Die 2 - BLE is a form of wireless communication designed especially for short-range communications.
**FAN-OUT IS SEEING ADOPTION IN SMARTWATCHES**

Leading OEMs: APE Fan-Out Packaging in Smartwatches

<table>
<thead>
<tr>
<th>Source: Samsung ePLP for the Exynos 9110 from System Plus Consulting</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SMARTWATCH</strong></td>
</tr>
<tr>
<td>Samsung Galaxy Watch</td>
</tr>
<tr>
<td>Exynos 9110</td>
</tr>
<tr>
<td>APU + PMIC</td>
</tr>
<tr>
<td>ePLP (Fan-Out)</td>
</tr>
<tr>
<td><strong>Packaging Process</strong></td>
</tr>
<tr>
<td>Package thickness (No bumps)</td>
</tr>
<tr>
<td>230um</td>
</tr>
<tr>
<td>660</td>
</tr>
<tr>
<td>74mm²</td>
</tr>
<tr>
<td><strong>I/O Density and Minimal LS have achieved advanced requirements with HD FO, be it at substrate level technology or wafer level technology.</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Source: Apple Watch Series 4 System in  package teardown from System Plus Consulting</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SMARTWATCH</strong></td>
</tr>
<tr>
<td>Apple Watch S4</td>
</tr>
<tr>
<td>A12 Custom</td>
</tr>
<tr>
<td>APU + Dummy Si</td>
</tr>
<tr>
<td>inFO_PoP (Fan-Out)</td>
</tr>
<tr>
<td><strong>Packaging Process</strong></td>
</tr>
<tr>
<td>Package thickness (No bumps)</td>
</tr>
<tr>
<td>199um</td>
</tr>
<tr>
<td>1092</td>
</tr>
<tr>
<td>118mm²</td>
</tr>
</tbody>
</table>

| **End-Application** |
| **Model** |
| **Chipset** |
| **Devices** |
| **Packaging Process** |
| **Package thickness (No bumps)** |
| **I/O** |
| **Package Area** |

**HD FO (Substrate)**

**Market Range**

**HD FO (Wafer)**
## VOLUME PRODUCTION ROADMAP FOR FOWLP

### Key parameters

Roadmap described here is for volume production, and provides an expected average of the different technologies on the market.

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Maximum package size</td>
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<tr>
<td>Side-by-Side Die</td>
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<tr>
<td>Max level of RDL</td>
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<td></td>
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<td></td>
<td></td>
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<tr>
<td>Min. Line/Space</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>Package minimum thickness (without BGA)</td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>Minimum die size (X–Y directions)</td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Maximum die size (X–Y directions)</td>
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<td></td>
<td></td>
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<tr>
<td>Minimum bump pitch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum die-to-die distance</td>
<td></td>
<td></td>
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</tbody>
</table>
Two main areas of focus for Fan-Out in Mobile/Telecom market, following two trends in technologies: **Core Fan-Out** & **HD Fan-Out**

‘Core Fan-Out’ exists for a large range of applications and will become widespread, taking market share of WLCSP and Flip-Chip with larger embedding capability. ‘HD Fan-Out’ appeared in 2016 for APE and will become widespread in high-end phones with more dies embedded, and potentially memories.
FAN-OUT PACKAGING TECHNOLOGY ROADMAP: DIFFERENT END-MARKETS

<table>
<thead>
<tr>
<th>Current Applications</th>
<th>Future Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Fan-Out</td>
<td>Exists in “Automotive &amp; Transportation” and “Medical”</td>
</tr>
<tr>
<td>HD Fan-Out</td>
<td>Not found in any other market apart from “Mobile &amp; Consumer”</td>
</tr>
<tr>
<td>UHD Fan-Out</td>
<td>Development</td>
</tr>
</tbody>
</table>

- New potential in “Automotive & Transport” - Sensors
- New potential in “Telecom & Infrastructure” - 5G
- Qualification: “Telecom & Infrastructure” - Data Centers and AI

*Future potential applications gathered from technical paper interest and interviews
## TSMC: New InFO technologies and summary

### Metrics

<table>
<thead>
<tr>
<th>PRODUCTION</th>
<th>inFO_PoP</th>
<th>inFO_oS &amp; inFO_MS</th>
<th>inFO_AiP</th>
<th>inFO_MiM</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRODUCTION</td>
<td>HVM since 2016</td>
<td>LVM since 2019</td>
<td>Qualification LVM expected in 2020</td>
<td>Qualification</td>
</tr>
<tr>
<td>STATUS</td>
<td>High-volume production of Gen-3</td>
<td>Successful qualification of multiple 16nm SoC chips. Better yield</td>
<td>Enables low transmission loss and high antenna performance for mmWave system</td>
<td>Validated better performance as compared to FC.</td>
</tr>
<tr>
<td>APPLICATION</td>
<td>Mobile APE+Memory: Smartphone, smartwatches, tablets</td>
<td>High Performance Computing: AI chips, servers; networking</td>
<td>mmWave wireless communication: 5G, Wi-Fi, modems, sensors</td>
<td>Advanced Mobile &amp; HPC</td>
</tr>
<tr>
<td>BENEFITS</td>
<td>Integrate systems with lower TTV as compared to FC, at finer L/S for board-level I/O</td>
<td>Enable better yield as compared to a single large die SoC</td>
<td>Enable low transmission loss and high antenna performance for mmWave system</td>
<td>Validated and simulated better performance and form factor as compared to FC and TSV.</td>
</tr>
</tbody>
</table>

### SCHEMATIC

- **Source:** “inFO_AiP Technology for High Performance and Compact 5G Millimeter Wave System Integration” TSMC: ECTC, 2018
- **Source:** “3D-MiM (MUST-in-MUST) Technology for Advanced System Integration” TSMC: ECTC, 2019

### Additional Information

- **inFO is leading APE packaging in mobile and continues to develop and penetrate new applications**
Deca’s validation of heterogeneous integration

Deca is focused on precision processing for finer LS with adaptive patterning.

New

Scaling Adaptive Patterning™ down to 2µm line & space and below

Source: Deca Technologies

Scaling M-Series™ up to 600mm panels

Large Panel 600mm x 600mm
After the successful completion of first FOPLP consortium, Fraunhofer IZM is currently organizing the second…

*PLC 1.0 (Completed)

In 2016, Fraunhofer IZM and partners launched PLC 1.0 to tackle FOPLP’s main challenges.

Full Members

- Unimicron
- AT&S
- Hitachi Chemical
- ASM Pacific Technology Ltd.
- evatec
- nanium
- breuer-science
- SEMSYSCO

Supply Chain Members

- ShinEtsu
- FUJIFILM
- SUSS MicroTec
- Mitsu Chemicals
- ATOTECH
- AJINOMOTO
- Meltex

*PLC = Panel Level Consortium

New

*PLC 2.0

Second consortium is still in progress as of 2019. It will be pre-competitive focused on exploring further details and physical limits of this technology. Deliverables include participation in research project steering and controlling and One-on-One technology transfer.
PTI, Nepes Laweh & Samsung Electronics have entered production in 2018. We are expecting these players to continue production through 2020.

ASE is expected to be running HVM by 2022.

Also ESWIN will potentially be the first FOPLP player in China to run LVM production by 2021.
Panel will progressively take a share of production but still in a limited way.

FOPLP is expected to take off at a much later time when big die applications are adopted.
YOLE GROUP OF COMPANIES RELATED REPORTS

Yole Développement

Advanced Packaging Quarterly Market Monitor

Equipment and Materials for Fan-Out Packaging 2019

Status of the Advanced Packaging Industry 2019

Contact our Sales Team for more information
Mediatek Autus R10 (MT2706) 77/79 GHz eWLB/AiP Radar Chipset

Fan-Out Packaging Processes Comparison 2020
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