

EQUIPMENT AND MATERIALS FOR 3D-NAND MANUFACTURING 2020

Market & Technology Report - November 2020

The 3D-NAND manufacturing equipment market will keep growing, propelled by robust long-term NAND-bit demand and ever-increasing manufacturing complexity.

KEY FEATURES

- 2019-2025 market forecast in units and revenue (US\$) for four types of equipment used for manufacturing 3D-NAND wafers, namely:
 - Dry etching – High Aspect Ratio (HAR) etching, hard-mask opening, resist trimming, conductor/dielectric etching
 - Deposition – Plasma Enhanced (PE) CVD and ALD for dielectric and conducting materials
 - Lithography – ArFi immersion and ArF, KrF, and I-line dry lithography
 - Hybrid bonding – wafer-to-wafer bonding such as YMTC's Xtacking™
- Analysis of 3D-NAND manufacturing materials, their technical requirements, trends, roadmaps, and key suppliers
- Description of technical trends and challenges in the 3D-NAND business, scaling roadmaps, along with overview of main players and product-development roadmaps.
- Mapping of the NAND supply chain, analysis of recent M&A and joint ventures, list of noteworthy news, and company announcements in 2019-2020
- Analysis of COVID-19's impact on the 3D-NAND business: effect on demand, bit shipments, and capex

ETCHING AND DEPOSITION WILL DRIVE THE GROWTH OF THE 3D-NAND MANUFACTURING EQUIPMENT MARKET

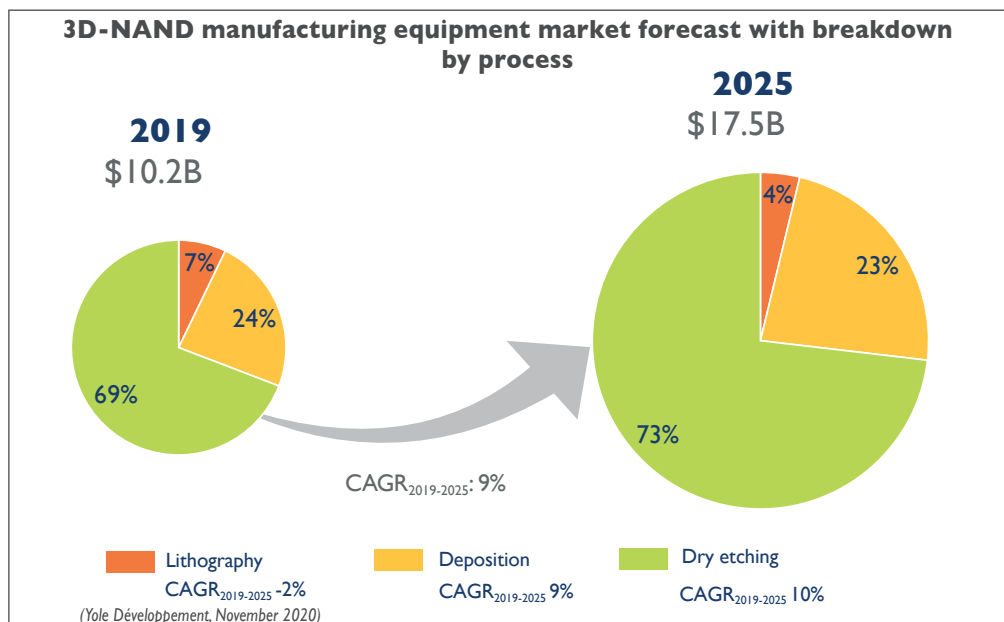
NAND Flash has become a mainstream technology because of its high scalability, which allows increased bit-density and lower cost-per-bit in next-generation storage technologies. Its adoption has been accelerated by extraordinary advances in the underlying manufacturing processes, which have enabled a major technological transition from planar 2D to 3D architectures and continuous scaling through vertical stacking of memory cells.

Despite some seasonality and cyclical, which are typical of the stand-alone memory business, the NAND market is expected to grow from \$44B in 2019 to \$81B in 2025 with a compound annual growth rate (CAGR₁₉₋₂₅) for this period of 11%. This will be driven by robust long-term bit demand fueled by rising data-centric applications in the fields of artificial intelligence (AI) and the internet of things (IoT), intelligent factories, virtual/augmented reality, and autonomous vehicles. In turn, the expansion of the NAND market will trigger new growth in the Wafer Fab Equipment (WFE) market, particularly in the areas of etching and deposition. In 3D-NAND, scaling occurs primarily in the vertical direction. Lithography requirements are therefore more relaxed compared to other memory technologies, whereas High Aspect Ratio (HAR) etching and thin-film deposition are critical.

In the next five years, the 3D-NAND equipment business will be further propelled by the continuous increase in manufacturing complexity and number of processing steps, which will boost equipment capital expenditure (capex) required for ramping up next-generation 3D-NAND nodes. Remarkably, 3D-NAND is an etch-intense technology, with more than 50% of the equipment capex required for etching.

The total 3D-NAND equipment market spanning etching, deposition and equipment is expected to reach \$17.5B by 2025. It will be driven by etching, with a CAGR₁₉₋₂₅ around 10%, and deposition, with a CAGR₁₉₋₂₅ around 9%.

Four companies – ASML, Applied Materials, Tokyo Electron and Lam Research – hold more than 70% of the overall equipment market. ASML is the unquestioned leader in the field of lithography. Lam Research is the market leader for etching and since 2011 and has also been expanding in the CVD/ALD segment. Applied Material, Tokyo Electron and Lam Research compete intensely in different areas, including CVD, ALD and PVD and etching. These three players will benefit most from expansion of the 3D-NAND business, but it will be also very sensitive to tail- and headwinds in the memory industry.



ADVANCES IN THE FIELD OF 3D-NAND MANUFACTURING ARE ENABLED BY BOTH EQUIPMENT AND MATERIAL DEVELOPMENTS

In the highly competitive 3D-NAND business, there is need for ad hoc tools capable of addressing complex challenges. Etching tools must drill deep

channel holes from the top of the device to the bottom substrate. Deposition tools must produce high-quality defect-free thin films with nanometer thicknesses. Metrology/Inspection tools are also becoming essential to monitor the processes and maintain high yields. Ideally, these challenging tasks need to be accomplished in the fastest possible time and lowest cost. In this framework, the competition among equipment suppliers to deliver the best solutions is growing fierce.

Besides equipment technology development, a great deal of R&D effort has to be focused on finding new material solutions. For instance, new hard mask materials with high selectivity like metal-doped carbides are being investigated intensely. So too are new metals for contact lines, alternative precursors for tungsten deposition, new channel materials to avoid charge mobility degradation, and more. Several material suppliers are involved in the 3D-NAND business and offer material solutions to challenging manufacturing steps, such as dielectric stack deposition or HAR etching.

Examples of technical challenges, material solutions and players*

STACK DEPOSITION

Deposited materials

- Alternating layers:
 - Silicon Oxide
 - Silicon Nitride

CVD precursors

- Silane+N₂O
- HCDS+ NH₃
- DCS+ NH₃
- TDMAS
- Disilane
- 3MS, 4MS

CVD precursors suppliers

Non exhaustive lists of companies and materials.

HAR HOLE ETCHING

Hard mask amorphous carbon

Etching chemicals

- CH₃F
- C₄F₆
- NF₃

Etching chemicals suppliers

**This analysis is available for all the process steps.*

(Yole Développement, November 2020)

SPECIFIC TECHNICAL STRATEGIES ARE NEEDED FOR NEXT-GENERATION 3D-NAND PRODUCTS

3D-NAND memory manufacturers will adopt different strategies to increase the number of layers and the overall bit density per die. There are three focus areas:

- 1) String-stacking. Whereas all players have already adopted a double-stack approach, Samsung – the industry leader – is the only player to develop the 128-layer generation with a single-string approach and thus enjoys higher margins on NAND than other chipmakers. For the following generation Samsung is expected to adopt double stacking.
- 2) Cell architecture. All the manufacturers except Intel have adopted the Charge Trap (CT) solution for their 1xx 3D-NAND technologies. Intel has recently announced the sale of its 3D-NAND business to SK hynix, and we expect they could shift from floating gate (FG) to CT as the deal with SK hynix moves forward. The transfer of the NAND business is expected to be completed by 2025.

3) Logic circuit position. Besides Micron, with circuit-under-array (CUA), SK hynix, with 4D NAND™, and YMTC, with Xtacking™, all players need to implement specific solutions to minimize the silicon-area consumption of the CMOS logic circuit.

Nowadays, all major 3D-NAND manufacturers are carrying out R&D activities to explore the use of wafer-to-wafer stacking approaches based on hybrid bonding. For instance, Samsung has not yet disclosed an approach to minimize the CMOS logic-circuit area and has a strong know-how in bonding technologies stemming from its CMOS Image Sensor (CIS) and High-Bandwidth Memory (HBM) businesses. It could be a potential candidate for the adoption of hybrid bonding for 3D-NAND. SK hynix could follow Samsung. In fact, although SK hynix already has CUA architecture 4D-NAND, it also has sound expertise in bonding for HBM and CIS and has recently licensed Xperi's 'DBI' technology for advanced memory applications.

Among the hybrid-bonding tool suppliers, EV Group has achieved a leading position in the field of 3D-NAND, and could benefit from a fast-growing market in the next 5 years (CAGR₁₉₋₂₅ of 20%) in the hypothesis that two major manufacturers will adopt hybrid bonding by 2023.

Leveraging extensive knowledge of the NAND business and related manufacturing equipment and processes, Yole is glad to introduce the brand-new report "Equipment and Materials for 3D-NAND Manufacturing". This report is the result of tight collaboration between Yole Développement and the reverse-engineering company System Plus Consulting, which performed a detailed analysis of the leading-edge 3D-NAND devices by all major memory suppliers.

Technology choices of leading 3D-NAND manufacturers

2019-2020	SAMSUNG	KIOXIA Western Digital	FLASH	SK hynix	YMTC
Number of layers	92L	96L	96L	96L	64L
Number of strings	1 string	1 string	2 strings	2 strings	1 string
Logic circuit position	CNA	CNA	CUA	CUA 4D NAND	Hybrid Bonding Xtacking™
Memory-cell architecture	CT	CT	FG	CT	CT

2020-2021	SAMSUNG	KIOXIA Western Digital	Micron	intel	SK hynix	YMTC
Number of layers	128L	112L	128L	144L	128L	128L
Number of strings	1 string	2 strings	2 strings	3 strings	2 strings	2 strings
Logic circuit position	CNA	CNA	CUA	CUA	CUA 4D NAND	Hybrid Bonding Xtacking™
Memory-cell architecture	CT	CT	CT	FG	CT	CT

CT = Charge Trap - FG = Floating Gate - CUA = CMOS Under Array - CNA = Circuit Next Arra
 *Non exhaustive list of companies

REPORT OBJECTIVES

Provide an overview of the stand-alone memory business with focus on NAND

- Present an overview of the wafer-fab equipment technologies and processes:

Deposition (CVD, ALD), dry etching, lithography, and hybrid bonding.

- Describe the 3D-NAND manufacturing equipment, materials, and processes
 - 3D-NAND architectures and technical trends: string stacking, circuit under array (CUA) vs. Xtacking™, and more
 - Technical challenges and equipment solutions for manufacturing 3D-NAND
 - Manufacturing materials: suppliers and technology/market trends.
- Provide market forecast for the period 2019-2025: revenue, ASP, and units
- Detail and analyze the competitive landscape:
 - Financial analysis of top NAND manufacturers and equipment suppliers
 - Latest company news, mergers, and acquisition

COMPANIES CITED IN THE REPORT (non exhaustive list)

ACM Research, Adeka, Advantest, AGC, Air Liquide, Air Products, Amec, Applied Materials, ASM International, ASML, Cabot Microelectronics, Canon, Coventor, Cypress, Dow, Dupont, Entegris, Enthone, Eugene Technology, EVG, Fujifilm, Fusion IO, GigaDevice, GlobalFoundries, Hansol Chemical, Heraeus, Hitachi Chemical, Hitachi High Technologies, Intel, JSR Corporation, Jusung Engineering, Kingston, Kioxia, KLA Tencor, Lam Research, Linde, Macronix, Materion, Merck, Micron, Mitsubishi Materials, Nanometrics, Naura, Nikon, Nippon Kayakli, Nova, Onto Innovation, Samsung, SanDisk, Screen, Seagate, Semes, Shin Etsu, SK hynix, SK materials, Smee, Spansion, Sumitomo Bakelite Co., Praxair, Rudolph Technologies, SMIC, Tok, Tokyo Electron, Teradyne, Tes, Toshiba, Tok, Tsinghua Unigroup, TSMC, Ultratech, UMC, UniC Semiconductors, Uyemura, Veeco, Versum, Western Digital, Winbond, Wonik IPS, Wonik Materials, XFab, XMC, Xperi, YMTC, Zeon, and more.

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Walt Coon joins Yole Développement's memory team as VP of NAND & Memory Research, part of the Semiconductor & Software division. Based in the US, Walt is leading the day-to-day production of both market updates and Market Monitors, and is deeply involved in the business development of these activities. Prior to Yole, Walt spent 16 years at Micron Technology. Walt Coon earned a Master of Business Administration from Boise State University (Idaho, United-States) and a Bachelor of Science in Computer Science from the University of Utah (United-States).

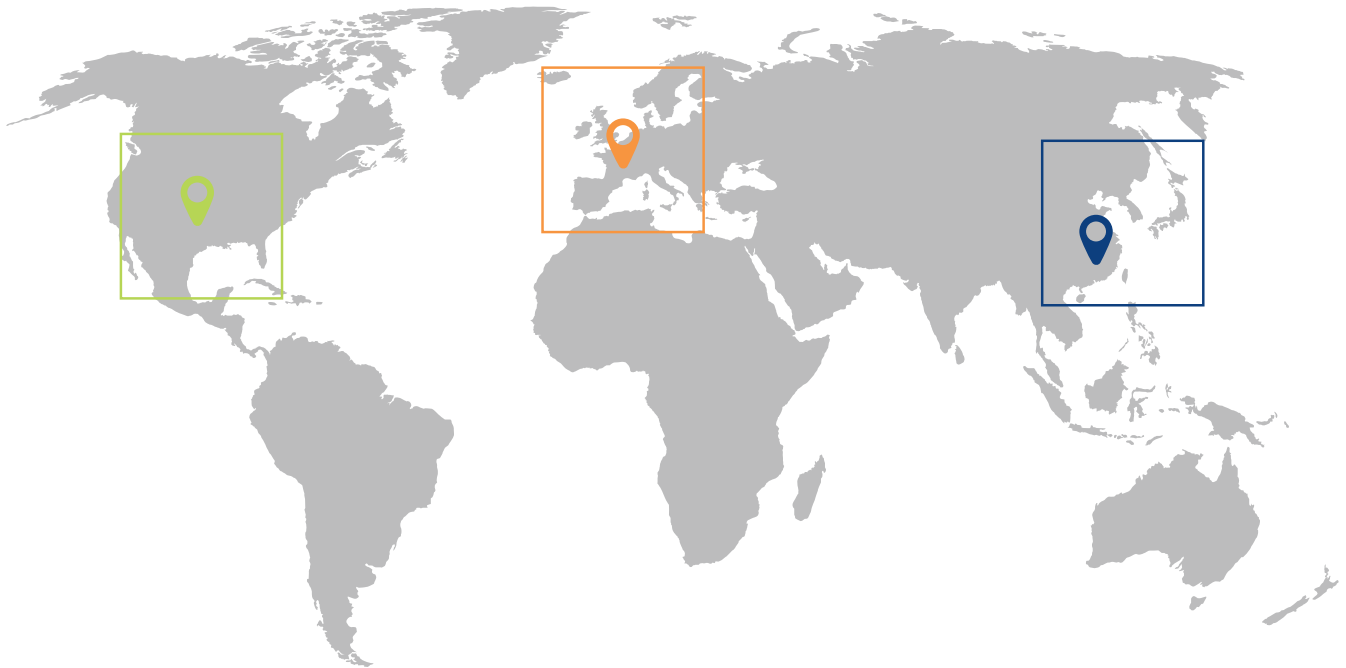
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Bank code: 30056
Branch code: 00170
Account n°: 0170 200 1565 87
BIC or SWIFT code: CCFRFRPP
IBAN: FR76 3005 6001 7001 7020 0156 587

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3.3 Payment is due by the Buyer to the Seller within 30 days from invoice date, except as otherwise specifically agreed in writing by the Buyer and the Seller. If the Buyer fails to pay at the due date and fails to request and obtain from the Seller a payment extension, the latter shall be entitled to invoice interest in arrears based on the annual rate Refi of the “BCE” + 7 points, in accordance with article L.441-6 of the French Commercial Code.

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6.7 It is further acknowledged and agreed by the Buyer that any investor in the Buyer Company, any external consultant of the Buyer Company or any joint venture done with a third party in which the Buyer Company is involved , is not entitled to use a Product, without paying to the Seller the full price for a license to the required Product..

7. TERMINATION

If the Buyer cancels the order in whole or in part or postpones the date of mailing, the Buyer shall indemnify the Seller for the entire costs that have been incurred as at the date of notification by the Buyer of such delay or cancellation. This may also apply for any other direct or indirect consequential loss that may be incurred by the Seller, pursuant to such cancellation or postponement.

8. MISCELLANEOUS

8.1 All the provisions of these General Terms and Conditions of Sale are for the benefit of the Seller, but also for that of its licensors, resellers and agents. Each of them is entitled to assert and enforce these provisions against the Buyer.

Any notices under these Terms and Conditions shall be given in writing and shall be effective upon receipt by the other Party.

8.2 The Seller may, from time to time, update these General Terms and Conditions of Sale, and the Buyer, shall be deemed to have accepted the latest version of such General Terms and Conditions of Sale, once they have been duly communicated to the Buyer by the Seller.

9. GOVERNING LAW AND JURISDICTION

- 9.1 Any dispute arising out or linked to these General Terms and Conditions of Sale or to any Licenses or Products purchased in application thereof shall be submitted to the French Commercial Court of Lyon, which shall have exclusive jurisdiction upon such issues.
- 9.2 French law (without reference to any applicable conflict of law provisions) shall apply to these General Terms and Conditions of sale and any agreement between the Buyer and the Seller made pursuant thereto.