

HIGH-END PERFORMANCE PACKAGING: 3D/2.5D INTEGRATION 2020

Market & Technology Report - November 2020

Intel Foveros and TSMC-SolC™ are competing head-to-head for high-end packaging - How will Samsung react?

KEY FEATURES

- Yole Développement's definition of high-end performance packaging
- High-end performance packaging market segmentation
- Market valuation based on top-down and bottom-up models in package units, revenue and wafer production volumes
- Market valuation of key high-end packaging technologies: 3D SoC, 3D stacked memory, 2.5D interposers, UHD FO, embedded Si bridge
- Includes COVID-19 impact on all forecasts
- High-end performance packaging market trends: end-system drivers
- Commercialization of high-end performance packaging products
- Global mapping of high-end performance packaging supply chain
- Supply value chain analysis in high-end performance packaging
- State-of-the-art technologies and trends
- Application technology roadmap of high-end performance packaging
- Key player's technology roadmap of high-end performance packaging: Intel, TSMC and Samsung
- IP analysis: 3D SoC – hybrid bonding

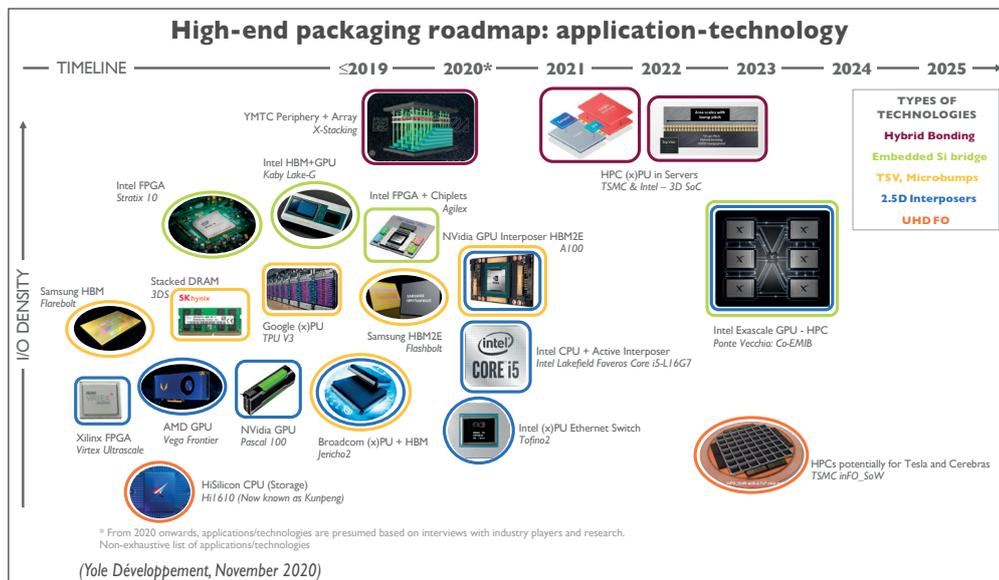
WHY IS HIGH-END PERFORMANCE PACKAGING'S ROLE INEVITABLY CRUCIAL TO THE SEMICONDUCTOR INDUSTRY?

Although Moore's Law has remained alive for over five decades, it is no longer cost-efficient. When it comes to advanced lithographic nodes, lesser manufacturers can keep up. Now there are only three leading-edge players, Intel, Samsung and TSMC. The industry is now diligently using advanced packaging technologies to put multiple advanced and/or mature chips in a single package, which is also known as heterogeneous integration. Together with 2.5D/3D packaging this extends Moore's Law at system-level.

Times have changed. The industry is seeking alternatives to design and manufacture the latest Systems on Chips (SoCs) using System in Package (SiP) and chiplet-based approaches by leveraging high-end packaging to mix both the latest and mature nodes. 2.5D/3D packaging is accelerating into new technical breakthroughs for 3D Interconnect Density (3D ID). Such

is the crucial role of high-end performance packaging in the semiconductor industry.

Prior to 2019, there has been very good traction for high-end packaging being commercialized in 3D stacked Dynamic Random Access Memory (DRAM), High Bandwidth Memory (HBM), Field-Programmable Gate Arrays (FPGA). It has been used in various processors including Central Processing Units (CPUs) and Graphics Processing Units (GPUs) in applications like processor cores, Solid State Drives (SSDs), memory blocks and graphics. Moving forward, more complexity and synergy of packaging technologies are expected for high performance computing (HPC) applications. For example, TSMC and Intel are working on hybrid bonding to package de-partitioned SoCs with Front-End (FE) capabilities. Intel and TSMC are working on big-scale chips processing with high input/output (I/O) density for high-end packaging applications.



MARKET FORECAST FOR HIGH-END PERFORMANCE PACKAGING

The high-end packaging market is valued at \$0.8B in 2019. It's projected to reach \$4.7B by 2025, with a Compound Annual Growth Rate (CAGR) of 32% from 2019 to 2025. In terms of package units, high-end packaging is projected to have a 38% CAGR, increasing from 204.5M Units in 2019 to 1409.2M Units in 2025.

The biggest market for high-end performance packaging comes from the telecom and

infrastructure end-market, accounting for more than 60% from 2019 to 2025. High-end packaging is expected to grow fastest in the mobile and consumer and automotive and mobility sectors, at 60% and 88% respectively.

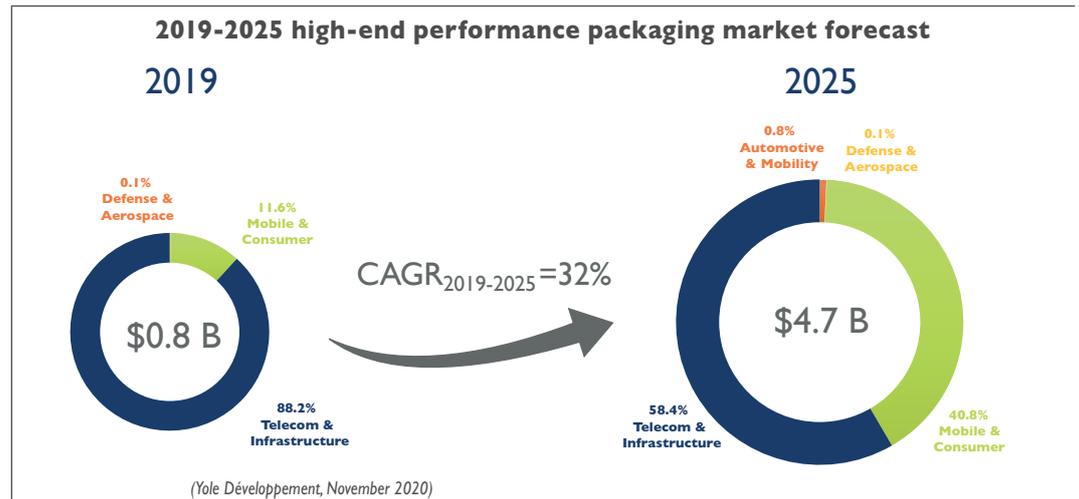
Among prominent digital age demands, high-end packaging drivers are coming from the increased implementation and interest of end-system units in cloud computing, networking,

HPC and consumer devices, personal computing and gaming. These key trends are paving the way for high-end packaging market opportunities.

In addition, the growth in consumer digitization and increase in adoption of internet of things, mobile connection and smart objects are expected to present major opportunities for the expansion of high-end performance packaging at the device level. They all need fast, big memory that interacts quickly with processing units. For example, in advanced computing for gaming, Through Silicon Vias (TSVs) are deployed in 3D

stacked DRAM and HBM. By equipping GPUs with high-speed memory, high-performance gaming can be achieved. Also, Apple has released its upgraded iMac pro that integrates the AMD Radeon GPU Vega 10 pro.

Although the market for high-end packaging in automotive and mobility is small, the growth rate is one of the highest. The strong growth of high-end packaging in this market is mainly attributed to the growing adoption of artificial intelligence and robotics in vehicles.



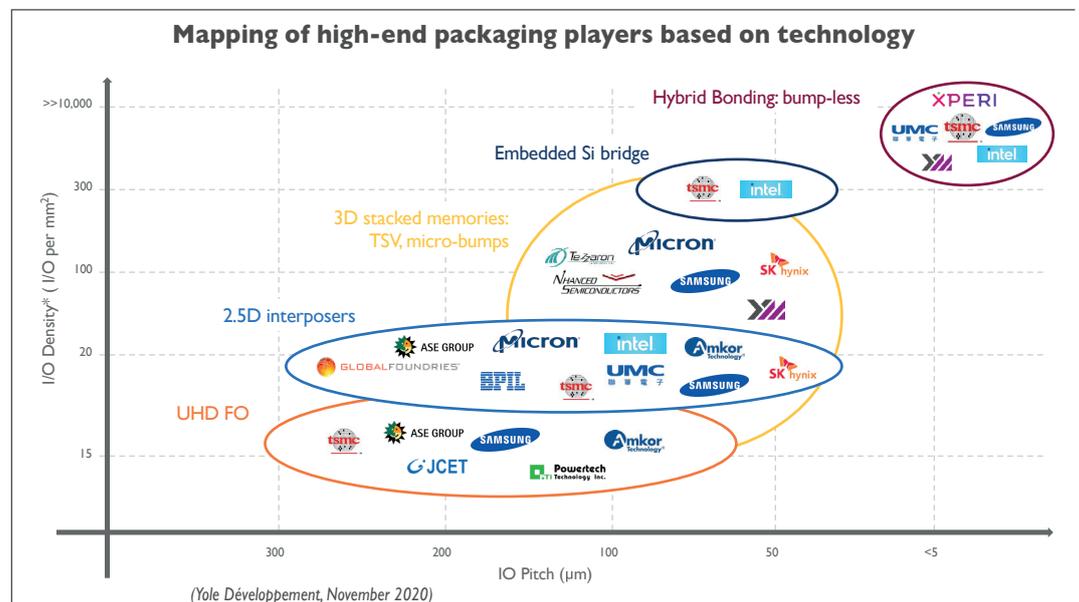
IMPACT OF BIG PLAYERS IN HIGH-END PERFORMANCE PACKAGING SUPPLY CHAIN

Wafer Level Packages (WLPs) are changing the standard Front-End (FE)/Back-End (BE) supply chain. A middle zone between FE and BE, where bumping and packaging can be executed on the wafer-level, can be reached by Outsourced Semiconductor Assembly and Test companies (OSATs), WLP houses and Integrated Device Manufacturers (IDMs).

Big players like Intel, TSMC and Samsung have successfully tapped into the advanced packaging market’s growth. They have achieved faster time-to-market than OSATs for high-end performance packaging, at historically unprecedented scale. This

strategy of big players poses a direct, formidable threat to OSATs.

Big players have both FE and BE capabilities. As a foundry, TSMC can be fundamentally focused on just FE and BE hence the new focus on 3D SoIC. So TSMC can make decisions quickly and follow through its strategy effectively. Intel has been actively promoting and commercializing its high-end packaging technologies like Foveros, EMIB and hybrid bonding for future roadmap. Intel’s Foveros is a direct challenge with TSMC’s CoWoS. Although Samsung is leading TSV for HBM, it is



not actively promoting logic 2.5D Interposers. Samsung and Intel need to ensure there is agreement from its design group all the way to system department. Any form of change is restricted by many locked-in legacies that slow down the progression for them to achieve a leading position in advanced packaging, which is typically viewed as risky and low priority.

Within high-end packaging, OSATs' business is being cannibalized by foundries and IDMs.

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Moving forward, the fabless model may become more attractive thanks to cutting-edge turnkey services, such as the latest silicon node manufacturing technology coupled with advanced packaging. Fabless companies and design houses are looking to optimized packages for value-for-money, especially for high-end applications. If big players can provide both quality and cost benefits, then OSATs may have to stay defensive in the existing packaging domain.

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REPORT OBJECTIVES

- To identify and describe which technologies can be classified as high-end performance packaging
- To define high-end performance packaging
- To analyze key market drivers, benefits and challenges of high-end performance packaging by application
- To describe the different existing technologies, their trends and roadmaps
- To analyze the supply chain and high-end performance packaging landscape
- To update the business status of high-end performance packaging technology markets
- To provide a market forecast for the coming years, and estimate future trends



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