Yole Développement

SYSTEM-IN-PACKAGE TECHNOLOGY AND MARKET TRENDS 2021

Market & Technology Report - July 2021

Through enabling design and supply chain agility, System-in-Package (SiP) will reach $19B by 2026, with IDMs, OSATs, and foundries taking advantage of it.

WHAT'S NEW

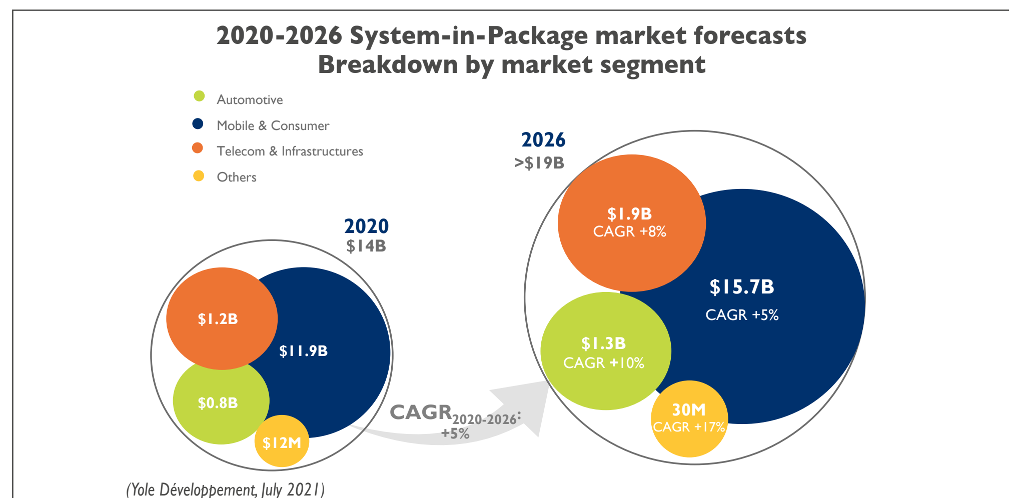
- Updated System-in-Package forecast from 2020-2026
- Updated System-in-Package supplier market shares
- Updated System-in-Package application mix
- Updated new RF modules & teardowns on SiP packaging structure
- Updated teardowns of latest mobile phones & analysis

KEY FEATURES

- System-in-Package market forecast by package units
- System-in-Package market breakdown (units & revenue)
- Combined System-in-Package forecast and market breakdown
- RF-SiP market in units and revenue
- Fan-Out SiP market forecast
- Embedded die SiP market forecast
- Flip chip/Wirebond SiP technology trends
- Fan-Out SiP key market applications

SYSTEM-IN-PACKAGE MARKET AND TECHNOLOGY OVERVIEW

SiP has become synonymous with technologies ranging from high-end die-to-die chiplet-type advanced integration to devices found in mobile handsets with increased integration and functionality leveraging best-in-class advanced packaging processes. The SiP platform is crucial in achieving 'More than Moore' in the race for heterogeneous integration, where advanced packaging remains at the forefront with front-end technology. This report provides an in-depth view of the SiP market by comprehensively discussing it in terms of mobile applications, computing applications, automotive, and high-end server applications. The SiP market is expected to increase from $14B in 2020 to $19B+ in 2026. The SiP product line includes high- to mid-end SiP devices, such as computing and data center applications, with much higher margins than the low-end SiP devices found in mobile handsets. High-end SiP is expected to grow at a CAGR of 9% from 2020 to 2026, whereas the low-end RF SiP found in mobile phones is expected to grow at a slightly lower CAGR of 5% from 2020 to 2026. In this report, SiPs are differentiated into three categories. These are the dominant flip chip/wire bond-based packaging form factors, Fan-Out based multi-die form factors, and embedded die form factors. The SiP remains a crucial platform as it allows the OEM customer to integrate one or more functionalities onto a substrate-based package instead of integrating it as a discret component on the PCB. The compact and miniaturized package is ideal for mobile handset devices. SiP provides flexibility and freedom to the designers in terms of sourcing the die and passive components for best-in-class cost and performance benefits. With the rise in SiP devices, many device wafers have adopted flip chip bumping or ball drop processes as these can be easily attached in SiP Packages, instead of using a wire bonding process to attach a die. WLCSP components have risen mainly due to the SiP platform's capability to integrate such varied form factors in a single package. In terms of technology and a roadmap, the SiP platform continues to push the boundary in the race to produce denser, thinner, and smaller form factors. These new process technologies include double-side molding technologies that eliminate the underfill operation from the bottom die resulting in an improved cost structure and manufacturing efficiencies. In addition to dual side molding, compartmental and conformal shielding remains another key process technology for RF-SiP devices. In terms of package height, OSATs are expected to push for 0.6 mm total package height for SiP devices in the coming years. With the deployment of 5G, increased development of materials is seen, to improve the reliability of SiP devices, especially in molding and solder ball materials. We can expect the industry to push the boundary of chip shooter tools to enhance the accuracy of component placing and throughput. In addition, we can also expect novel, reliable packaging materials to set the stage for the next set of SiP devices to drive heterogeneous integration further.



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SYSTEM-IN-PACKAGE SUPPLY CHAIN FOR LOW-END AND HIGH- TO MID-END SIP DEVICES

The global supply chain for SiPs has become complex as it spans IDMs, OSATs, and foundries. The low-end SiP business, such as RF SiPs, is dominated by top OSATs such as ASE w/SPIL, Amkor, and JCET, while Apple remains one of the biggest drivers for SiP momentum in the low-end SiP space for smartphone applications. Amkor has invested in the SiP platform with capex specific to SiP as it declared $700M estimated total capex for FY 2021, marking this one of the biggest capex years in the last 4-5 years. Amkor's SiP business is expected to grow 20-30% as it expands its capability in its Korean manufacturing plants. Amkor is not alone in enjoying SiP business growth, as ASE, with SPIL and USI, is also enjoying significant growth in its SiP product lines. ASE is competing with low-end SiP solutions where EMS capabilities can play a role, and also as an OSAT-based SiP business mainly targeting RF front-end applications and 5G chipset growth. An interesting development has surfaced in the evolution of the RF Antenna-in-Package - value-add services from OSATs, such as dual-side assembly, dual-side molding, and partial and conformal shielding with many passive components, has increased the package price resulting in a larger revenue stream for the OSATs. Given the breadth of the SiP demand, however, the market remains consolidated and dominated by a few top OSATs as they can offer the best device cost, scalability, and reliability. The business remains fiercely competitive and inhibits new entrants with less capacity, capability, and experience.

2017-2025 SiP technology roadmap - key parameters

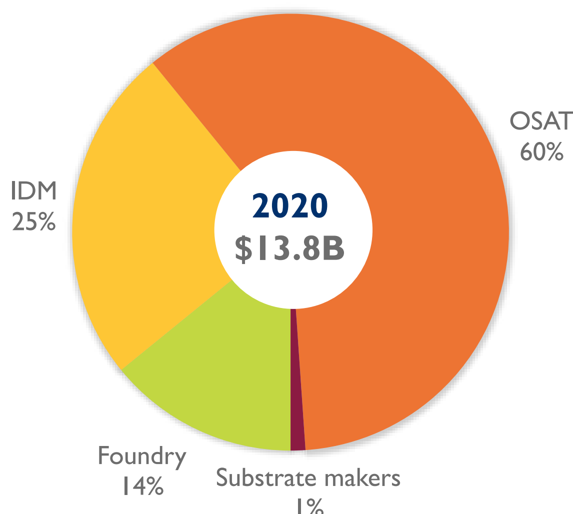
	Metrics	<2017	2019	2022	2025	SiP Advancement
Flip Chip (IC Substrate)	Substrate RDL L/S	30/30 to 10/10 µm	10/10 to 5/5 µm		8/8 to 5/5	FC BGA SiP
	Substrate I/O Pitch	1200 to 350 µm			300 µm	
	Substrate I/O Ball	500 - 3000		>> 3000		
	Max Package Size	> 65x65 mm		>> 80x80 mm		Double-Sided FC SiP
	Max no. of Dies/Passives	< 15	< 35	>> 35		
	Max level of RDLs	10 -16x RDL		>> 10x RDL		
Fan-Out	Substrate RDL L/S	15/15 to 8/8 µm	5/5 ! m to 2/2 µm		< 1/1 µm	FO on Substrate
	Substrate I/O Pitch	400 µm	350 µm	200 µm		
	Substrate I/O Ball	< 300	600 -1300	>> 1500		
	Max Package Size	< 5x5 mm	< 25x25 mm		< 30x30 mm	HD FO SiP PoP
	Max no. of Dies/Passives	≤ 2	≤ 4	≤ 6		
	Max level of RDLs	3x – 4x RDL		> 4x RDL		
Embedded Die	Substrate RDL L/S	> 25/25 µm	> 20/20 µm		> 15/15 µm	Embedded Interconnects
	Die I/O Pitch	250-80 µm		50 µm		
	Die I/O Numbers	40-100	100-150		150-200	
	Max Package Size	<15x15 mm		< 25x25 mm		Embedded Multi-Dies
	Max no. of Dies/Passives	≤ 2	≤ 3		≤ 4	
	Max level of RDLs	2x - 4x RDL		4x – 6x RDL		

(Yole Développement, July 2021)

Regarding Fan-Out SiP, TSMC maintains its dominance with the InFO-x product line for mobile and server applications. JCET and ASE w/ SPIL also have a healthy mix of multi-die Fan-Out modules for high-end applications. The Fan-Out SiP package market is expected to grow at 6% CAGR, becoming a $1.6B+ market by 2026. Similar to Fan-Out SiP, the Embedded SiP form factor is supported by niche players such as TDK, Semco, and ASE as it offers a number of benefits compared to the traditional flip chip-based approach, such as smaller package footprint, better signal delivery, and better heat management, and is well-suited for power delivery applications. Embedded die SiP packages are expected to gain momentum in the next few years, especially in the automotive sector.

EVOLUTION AND EMERGENCE OF NEW BUSINESS MODELS FOR SYSTEM-IN-PACKAGE PRODUCTS

2020 total SiP market share: packaging revenue, business model*



*Speculated breakdown, not final
*Data is generated by secondary research and revised through interviews

(Yole Développement, July 2021)

SiP global business models have evolved significantly over the past five years. OSATs have dominated in the past, and the demand was somewhat scattered in the SiP landscape 5-8 years ago. However, with mobile handsets, RF evolution, and 5G deployment, SiP has come of age and can robustly support multiple markets, starting with the low-end RF SiP markets dominated by top OSATs and driven by leading OEMs, such as Apple and Samsung. The high-end SiPs remain on a higher growth trajectory with post-pandemic demand accelerating infrastructure spend globally. This explosion in multiple segments has prompted IDMs, Foundries, EMS houses, and OSATs to compete in this thriving market. ASE's USI generates a significant portion of ASE's revenue and will approach 50% of the revenue in a few years. OSATs are developing capabilities to mount anywhere from 50-100 passive SMT components and manage a supply chain that was foreign to them just a few years ago. IDMs, such as Intel and Samsung, are driving hybrid die-to-die interconnect-stacked-packaging, such as Intel's

Foveros architecture and Samsung's x-cube architecture. These die-to-wafer or die-to-die interconnects will gravitate towards hybrid bonding, improving device performance and bandwidth in a near future. Intel is also targeting a Co-EMIB server product on 7 nm node by 2023. These advances in the high-end SiPs are here to stay, and increased M&A is expected within the top IDMs and foundries to increase their capabilities to develop these product lines in the best cost/performance envelope.

REPORT OBJECTIVES

- Describe technologies that can be classified as "System-in-Package"
- Identify and detail the System-in-Package platform's key process steps
- Analyze the supply chain for System-in-Package technologies
- For these steps, provide a market forecast for the coming years and a prediction of future trends

COMPANIES CITED IN THE REPORT (non exhaustive list)

Access, Amkor, Analog Devices, Apple, ARM, ASE, Avago, AT&S, Bosch, Broadcom, Carsem, China WLCSP, Chipbond, ChipMOS, Cisco, Continental, Cyntec, Cypress Semiconductor, Deca Technologies, Dyconex, Facebook, Fitbit, Flexceed, Flip Chip International, Formosa, Fraunhofer IZM, Freescale, Fujikura, Fujitsu, GaN Systems, General Electric, GlobalFoundries, Google, Hana Micron, Hella, Huawei, IMEC, Inari Berhad, Infineon, Intel, J-Devices, JCET, King Yuan, Lenovo, Linear Technology, LB Semicon, MediaTek, Medtronic, Meiko, Microchip, Microsemi, Nanium, Nepes, Nvidia, NXP, Nokia, ON Semiconductor, Orient Semiconductor, Powertech Technology Inc, Renesas, QDOS, Qorvo, Qualcomm, Rohm, Sarda Technologies, Samsung Electronics, SCC, Schweizer, SEMCO, SIMMTECH, SK Hynix, Shinko, ShunSin, SiPlus, Softbank, SONY, SPIL, Spreadtrum, STMicroelectronics, STATS ChipPAC, STS Semiconductor, Taiyo Yuden, TDK, Teraprobe, Texas Instruments, Tianshui Huatian, Tongfu Microelectronics, Tong Hsing, Toshiba, TSMC, Unimicron, Unisem, USI, UTAC, Wurth Electronics, and many more.

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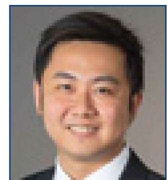

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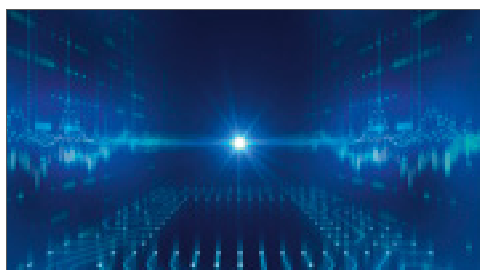

- Fan-Out WLP and PLP Applications and Technologies 2021
- 5G Packaging Trends for Smartphones 2021
- Fan-Out Packaging Processes Comparison 2020
- HiSilicon Hi1382 Coherent Processor with ASE's FOCoS
- Advanced System-in-Package Technology in Apple's AirPods Pro

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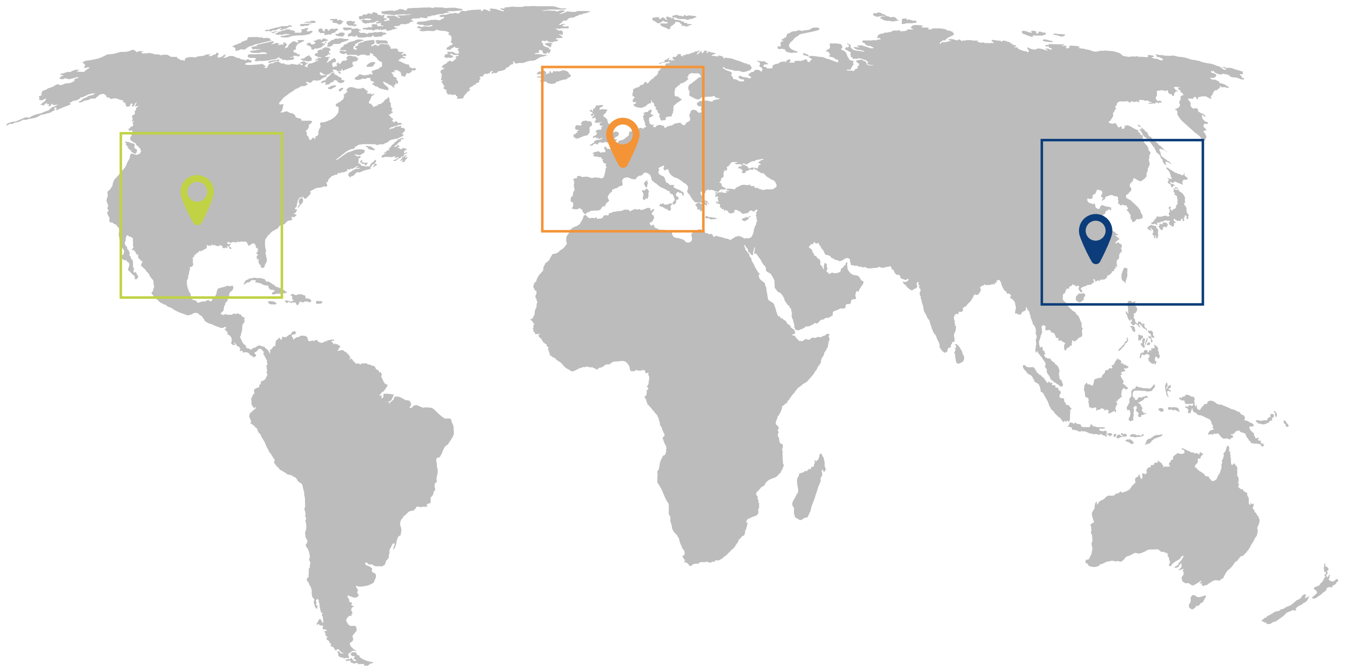

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