Apple M1 Max System-on-Chip

Full analysis of the Apple-developed 10-core CPU plus 32-core GPU processor for MacBook Pro. The precursor of the remarkably powerful Apple M1 Ultra SoC.
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## System Plus Consulting Services

Full report pages: 149
Biographies of the Authors

**Ying-Wu Liu, Technology & Cost Analyst**

Ying-Wu Liu serves as a Technology & Cost Analyst at System Plus Consulting, part of Yole Développement. Ying-Wu ‘s core expertise is Integrated Circuits technologies.

With solid expertise in physical and electronical analysis of devices and experiences in wafer manufacturing and technical supports with international clients, Ying’s mission is to develop reverse engineering & costing reports.

Prior to System Plus Consulting, Ying worked as Technical Support Manager at KEOLABS, where she had the opportunity to build up her ability to cooperate with clients from different cultures.

Ying holds a master’s degree in Theoretical Physics from the National Tsing Hua University (Taiwan), and a master in Integration, Security and Trust in Embedded systems from the Grenoble INP, ESISAR (France).

**Don Scansen, External Analyst**

Don Scansen has partnered with System Plus Consulting to launch the new die architecture and front-end process analysis of advanced SoC devices including APU, CPU, GPU, and FPGA. Don previously supported clients ranging from individual patent owners to Fortune 500 companies providing competitive analysis and intellectual property support. He holds a PhD in electrical engineering.

**Véronique Le Troadec, Laboratory Analyst**

Véronique Le Troadec serves as Senior Microelectronics Laboratory Senior Analyst at System Plus Consulting, part of Yole Développement.

With an extensive knowledge in failure analysis of components and in deprocessing of integrated circuits, Véronique’s mission is to oversee the physical analyses of electronic components, choose the operating mode adapted to the component to analyze and perform complex sample preparation and analysis by optical and electronic microscopy to deeply analyzing the structures.

She is also developing new methods of analysis on latest sub-nano node design and shares her experience with the other members.

Prior to System Plus Consulting, Veronique has worked for twenty years at Atmel as a component reliability technician. She was in charge of failure analyzes on automotive products, mainly microcontrollers. She also participated to the R & D projects.

She holds a University Diploma in physical measurements from the IUT of Lannion.
Executive Summary

While x86 architecture is still expected to account for most PC processing, Apple's switch to in-house processor silicon signals a major shift in this structure. Yole's market analysis expects 14% of PCs to run on non-x86 processors by 2027, up from just 4% in 2020. Apple's strategy with the M1 family and its derivatives is the main factor in this market shift, as Apple shows what is possible at the high-end of PC performance.

This full reverse costing study was conducted to provide insight on the technology data, manufacturing cost, and selling price of the Apple M1 Max System-on-Chip (SoC).

In 2020, Apple published the M1 SoC to run its macOS on a proprietary design. The birth of Apple’s first processor for personal computing created a shockwave in the industry. Apple became totally independent in processor development, leaving many to speculate whether the end of Apple sockets for Intel processors had arrived. The following year, Apple presented M1 Pro and Max SoC as the next generation of M1. Once again, Apple showed its ambition and capability with these two powerful SoCs. The M1 Pro’s die is twice the size of the M1’s die, and the M1 Max die is almost four times bigger.

According to Apple, the biggest and most powerful chip for Pro Notebook – M1 Max SoC – includes 57 billion transistors, which is 70% more than M1 Pro and 3.5 times more than M1. Regarding chip architecture, the M1 Max is equipped with a 10-core CPU, a 32-core GPU, a 16-core neural engine, and an Apple-designed media engine that boosts video processing while maximizing battery life. The chip is fabricated by TSMC on 5nm process, which is also used to manufacture Apple’s A14, A15 SoC, and the other M1 variants.

The Apple M1 Max SoC integrates four external LPDDR5 SDRAMs into a SiP (system-in-package). The SoC die is flip-chip mounted onto the M1 Max SoC PCB by ball grid array (BGA) and shares the same PCB with LPDDR5 SDRAM packages. The package also includes MLCCs (multilayer ceramic capacitors) and IPDs (integrated passive devices).

To reveal all the details of the Apple M1 Max SoC, this report features multiple analyses. These include a front-end construction analysis to reveal the most interesting features of the TSMC 5nm process, as well as package assembly and structure. In addition to a complete construction analysis using SEM cross-sections, material analyses, and delayering, we show high-resolution TEM cross-section images of TSMC’s 5nm features. A CT-scan (3D X-ray) is also provided to reveal the layout structure of the whole chip package. Moreover, the floorplan of the SoC die is included to give a clear view of IP blocks and general chip architecture. Lastly, this report contains a complete cost analysis and a selling price estimation of Apple’s M1 Max SoC.
Methodology & Key Features

Teardown analysis
- Package is analyzed and measured. The dies are extracted in order to get overall data: dimensions, main blocks, pad number and pin out, die marking.
- Setup of the manufacturing process

Costing analysis
- Setup of the manufacturing environment
- Cost simulation of the process steps

Selling price analysis
- Supply chain analysis
- Analysis of the selling price

REPORT’S KEY FEATURES
- Detailed photos
- Precise measurements
- Front-end structural analysis with TEM
- Back-end structural analysis with CT-scan
- Floor Plan
- Materials analysis
- Manufacturing process flow
- Supply-chain evaluation
- Manufacturing cost analysis
MacBook Pro Teardown

Physical Analysis
- Teardown
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FEOL (TEM Analysis)

Floor Plan

Manufacturing Process Flow

Cost Analysis

Selling Price Analysis

Feedback

Related Analyses

About System Plus
Apple M1 Max SoC Package Dimensions

- Apple M1 Max SoC:
  - Package type:
  - Area:
  - Thickness:
  - Pitch:
CT-Scan Images – Cross-section

Apple M1 Max SoC Package – CT-Scan Cross-section

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Package Cross-Section – Copper Pillar & SoC Solder Ball

- The SoC solder ball uses a based compound.
- is used between the metal layer of M1 Max SoC PCB.

Package Cross-sectioning – Optical View
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The memory package teardown reveals the LPDDR5 chips joined to the package substrate.
SoC Die Overview & Dimensions

- Die area:
- Nb of PGDW per 12-inch wafer:
- Pad number:

Apple M1 Max SoC Die – Overview
©2022 by System Plus Consulting
SoC Die Process – Technology Node

- The process uses FinFET transistors.
- Fin pitch: [nm]
- Gate pitch: [nm]
  - Estimated technology node: 35nm FinFET process
SoC Die Cross-Section – Metal Layers

The die process uses 6 metal layers:

- Polyimide
- Passivation

Apple M1 Max SoC Die – Overview
©2022 by System Plus Consulting

SystemPlus 15.0kV 15.9mm x6.0k SE(L)
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Apple M1 Max SoC Die Metal Layers – Overview
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TEM EDS Along PMOS Fin

The thickness of the sample cut along the fin major axis includes a portion of the gate materials.

A thicker portion exists above the fin.

Detailed analysis of the gate and dielectric stacks are not part of this report. The top to bottom stack of materials as indicated by the 2D maps is...
Die Floorplan – Major IP Block Area Description

- The Apple M1 Max application processor SoC floorplan was analyzed. The main IP blocks are shown in the figure at right.

- The largest contiguous circuit block is the GPU SRAM Cache and Control with an area of \_
  \_
  \_
  which accounts for \_
  \_
  \_
  of the design space inside the scribe seal boundary.

- The second largest block on the die is virtually identical in size at \_
  \_
  \_
  The General Purpose IO - A block occupies a wide swath of the entire left-hand edge of the die as shown at right. The third largest is also almost identically sized. There are two system-level SRAM caches above and below the graphics processor (GPU) area. Each of the L3 SRAM Cache Blocks A and B are \_
  \_
  \_
  mm\(^2\) and consume \_
  \_
  \_
  of the design area.

- Much of the die circuitry is devoted to unattributed general logic function. Logic – B is the largest of these at \_
  \_
  \_

- The largest area that includes smaller cores is the GPU, which is a total of \_
  \_
  \_

- The main computing of the M1 Max SoC is built on a ten-core architecture including eight high-performance HP CPU Cores as well as two low power Eff CPU Cores.
## Apple M1 Max SoC – Wafer Front-End Cost

<table>
<thead>
<tr>
<th>Front-End</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Raw wafer Cost ($)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clean Room Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equipment Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Consumable Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Labor Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield losses Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The **wafer front-end cost** for the Apple M1 Max SoC ranges from [ ] to [ ] according to yield variations.

We consider a gross margin of 52% for TSMC foundry which result in front end price in the range of [ ].

The largest portion of the manufacturing cost is due to the [ ] for medium yield.
Apple M1 Max SoC – Die Cost

<table>
<thead>
<tr>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Front-End Cost</td>
<td>BE : Probe Test Cost</td>
<td>BE : Bumping Cost</td>
</tr>
<tr>
<td>Total Wafer Cost</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Nb of potential dies per wafer
Nb of good dies per wafer

By adding the bumping, probe test, backgrinding & dicing cost, the Apple M1 Max SoC die cost ranges from according to yield variations.

The number of good die per wafer is estimated to range from according to the yield variations, which result in a die cost ranging from.
## Apple M1 Max SoC – Packaging Cost

### Package Manufacturing Cost Breakdown (Medium Yield)

<table>
<thead>
<tr>
<th>Component</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Substrate Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IHS Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FeCr Metal Frame Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clean Room Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equipment Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Consumable Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Labor Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield losses Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OSAT Gross Profit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Manufacturing Invoice from OSAT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield losses Cost absorbed by OEM</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The panel size is 123.45 mm.

The **packaging cost** is estimated to be in the range of 123.45 ± 0.05, according to yield variations.

The largest portion of the manufacturing cost is due to the **PCB substrate cost** at 45.67% for medium yield.

We estimate gross margin of 50.00% for the OSAT, which results in a **packaging price** ranging from 123.45 to 123.46.
## Packaging Cost per Process Step

### M1 Max SoC Die Deposition

<table>
<thead>
<tr>
<th>Process Operation</th>
<th>TOTAL COST (USD / Unit)</th>
<th>Breakdown</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPD Capacitor - Pick &amp; Place</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IPD Capacitor - NCP Underfill Deposition</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IPD Capacitor - Underfill Curing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Solder ball - Ball Dropping</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Solder ball - Solder Reflow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die - Pick &amp; Place</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die - Solder Reflow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die - CUF Underfill Deposition</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die - Underfill Curing</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total Cost</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SIP Assembly

<table>
<thead>
<tr>
<th>Process Operation</th>
<th>TOTAL COST (USD / Unit)</th>
<th>Breakdown</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory - Pick &amp; Place</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory - Solder Reflow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory - CUF Underfill Deposition</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory - Underfill Curing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MLCC - Pick &amp; Place</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Solder Reflow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Adhesive Deposition for Metal Frame</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal Frame - Pick &amp; Place</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Adhesive Curing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIM 1 Deposition</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Adhesive Deposition for IHS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IHS - Pick &amp; Place</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Adhesive Curing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIM 2 Deposition</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Curing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package - Dicing : Mechanical Saw</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total Cost</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Apple M1 Pro SoC Component Cost

The **component cost** is estimated to be in the ranges from [ ] according to yield variations.

The largest portion of the manufacturing cost is the **die cost at [ ]** for medium yield.

The packaging accounts for [ ] for medium yield.

The final test and yield losses account for [ ] for medium yield.

*We don’t consider any discount on DRAM and capacitor price. The actual price sold by the vendors to Apple could be lower.*
By System Plus Consulting:
- Apple M1 Pro System-on-Chip
- Apple A15 Bionic SoC
- Apple M1 System-on-Chip

By System Plus Consulting:
- Apple MacBook Pro 14-inch (2021)

By Yole Développement:
- Processor Quarterly Market Monitor

Contact us for more information
Our Core Activity: Reverse Costing®

A Technology, Process and Cost Analysis

Reverse Costing® consists of disassembling a device or a system in order to identify its technology and discern its manufacturing processes and then using in-house models and tools to determine its cost.
Fields Of Expertise

- **Electronic System**
  - Automotive
    - ADAS
    - Electrification
    - Infotainment
    - Telematics
    - Other ECUs
  - Consumer
    - Phone
    - Smart Home
    - Wearable
    - Tablet, Computing & Gaming

- **Semiconductor Device**
  - Battery
  - Compound Semiconductor
  - Computing and Software
  - Display
  - Emerging Technologies
  - Imaging
  - Memory
  - Photonics and Lighting
  - Power Electronics
  - Radio Frequency
  - Semiconductor Manufacturing
  - Semiconductor Packaging
  - Sensing and Actuating

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Company Profile
Physical Analysis
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Our Offers

- **Report**: 60+ per year
- **Monitor**: 1 per year quarterly updated
- **Teardown Track**: 205+ teardowns per year
- **Custom Analysis**: 150 custom analyses per year
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- **Cost Methods Training**: On demand
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